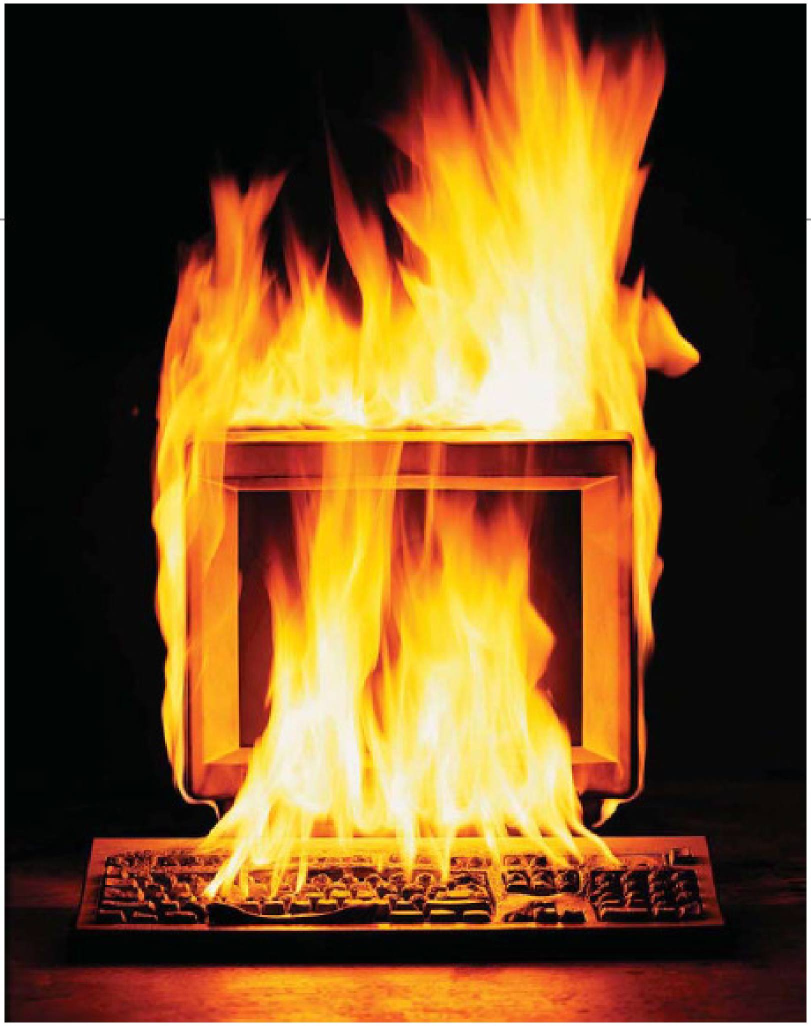
SELF-HEATING EFFECTS IN SOI DEVICES AND GAN HEMTS

Dragica Vasileska, ASU

Thanks to …

Katerina Raleva, Stephen M. Goodnick, Arif Hossain, Balaji Padmanabhan, Mihail Nedjalkov, David K. Ferry, Frank Schwierz



Computing's Power Limit Demonstrated

Fifty-year-old principle is proved: Erasing information gives off heat

Physicists in Europe have experimentally demonstrated, for the first time, that a theoretical principle limiting modern-day computing is real.

In 1961, Rolf Landauer posited that the act of erasing a bit of information gives off an amount of heat equal to problem, arguing that the energy wasn't free because the demon had to erase a bit of information in its memory in order to sort each particle.

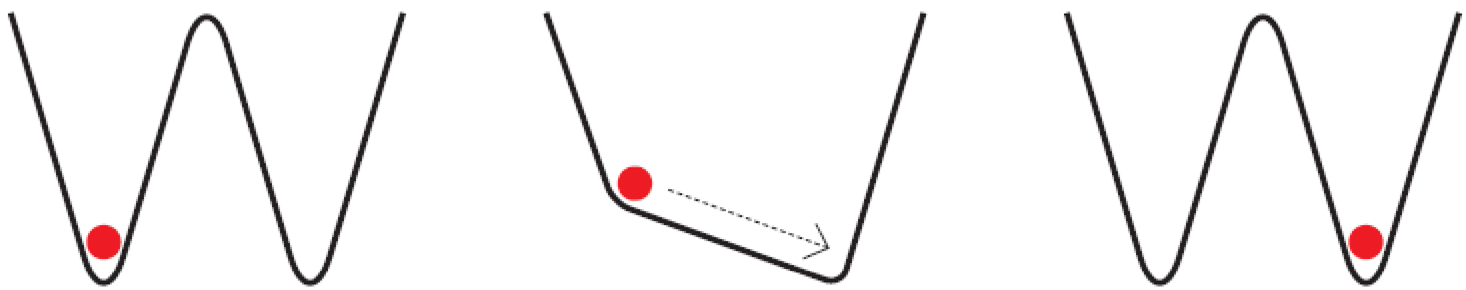
Though it sounds like a philosophical argument, the theory has real implications for computing. And the debate over its validity, some researchers claim, has influenced the direction of computing and semiconductor research.

Eric Lutz, who was at the University of Augsburg when the research was conducted, and a group of European scientists set out to demonstrate Landauer's limit by building his thought experiment in a real system. Landauer had imagined a memory consisting of a single particle. The particle called optical tweezers. The tweezers are a laser system that holds particles in place at the laser's focal point. The researchers made the two wells by alternating the focus between two points. Erasing the bit involves first manipulating the laser to

"This is beautiful experimental work," says IEEE Fellow Mark Lundstrom, a professor of electrical and computer engineering at Purdue University, in West Lafayette, Ind., and an expert on the limits of nanodevices.

Thought Experiment: Ralph Landauer

Dissipated Energy = $k_B T \ln 2 = 3 \times 10^{-21}$ Joules



SIMPLE MEMORY: Erasing a bit involves lowering the energy barrier between two states and forcing the system into one state.

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Outline

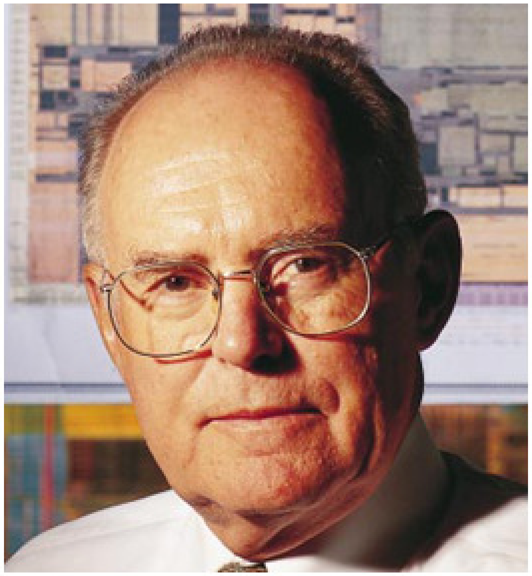
- Motivation
- Thermal Effects
- Previous Work Done in Thermal Modeling
- The ASU Model for Addressing Self-Heating
- Conclusions

Motivation

Transistor Scaling

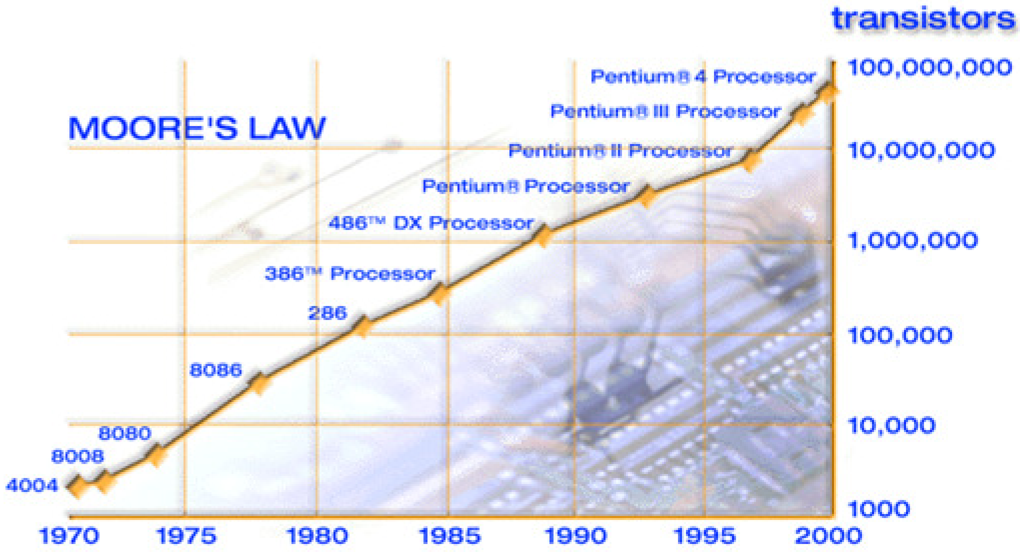
Thermal Effects and Scaling

Transistor Scaling: Moore's Law



Gordon Moore

"every 1.5 years complexity doubles"



www.intel.com

Transistor Scaling: Dennard's Law

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	Scaling K : K=0.7 for example
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor $\rightarrow$ In the past, $\alpha > 1$ for most cases
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ $= 1/K^2$, when $\alpha = 1$
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2}) K (K^1)^2 = \alpha$ $= 1$, when $\alpha = 1$

R. **Dennard**, et al., *IEEE Journal of Solid State Circuits*, vol. SC-9, no. 5, pp. 256-268, Oct. 1974.

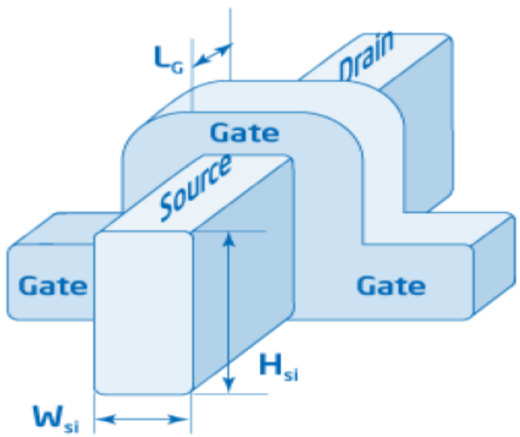
More Moore …

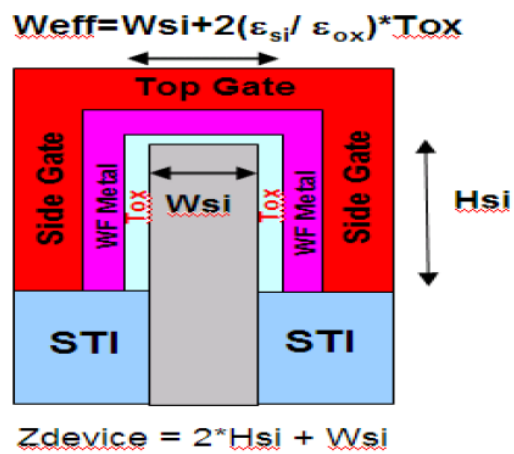
Multi-Gate Transistors Implementation

Multi-Gate Fin Transistor:

++ Self Aligned structure for S/D

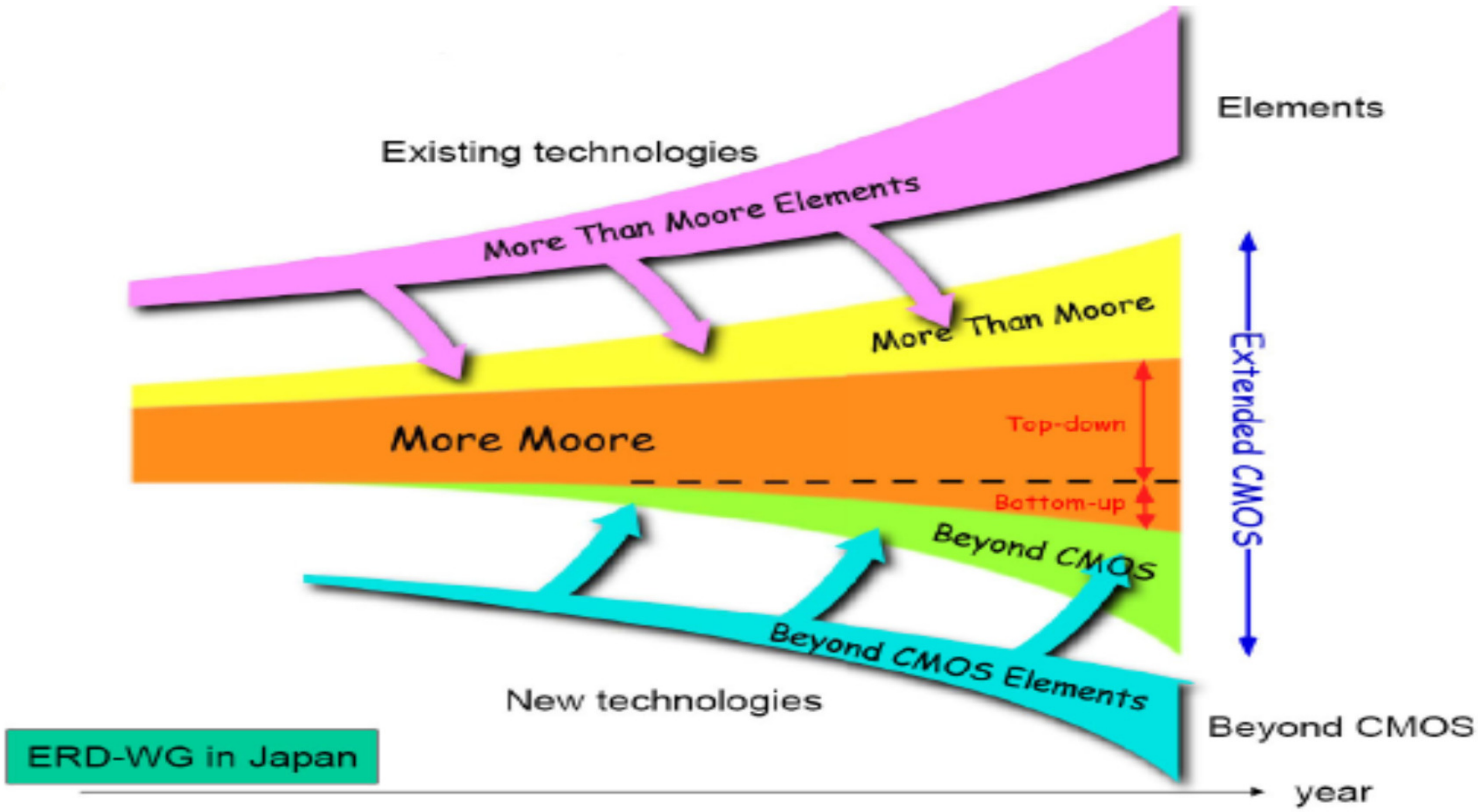
-- Non-Planar structure





Multi-Gate Fin Transistor

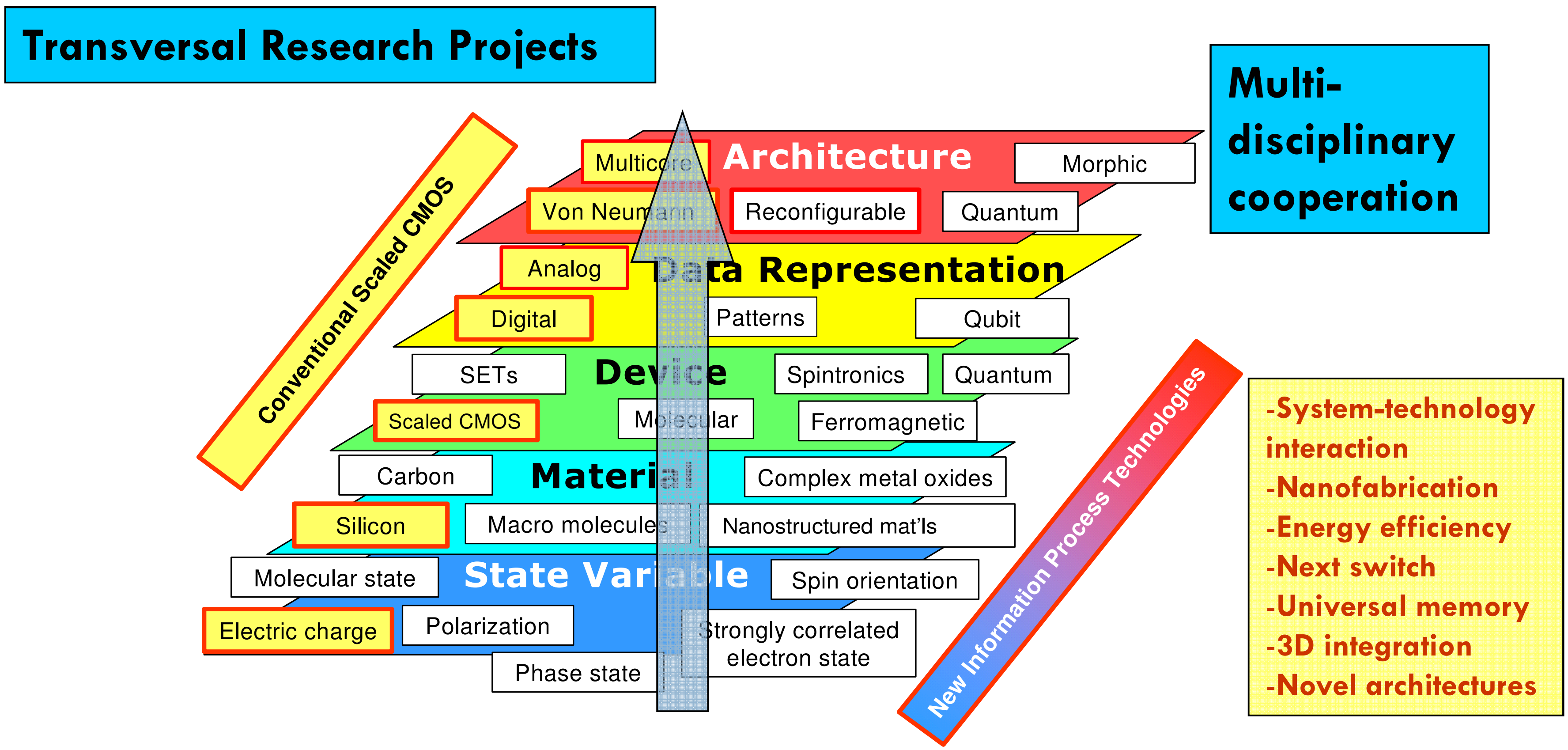
More Than Moore and Beyond CMOS



ITRS-ERD vision of the role of Beyond CMOS and More than Moore elements to form future extended CMOS platforms (2010).

www.itrs.com

2020 and Beyond …

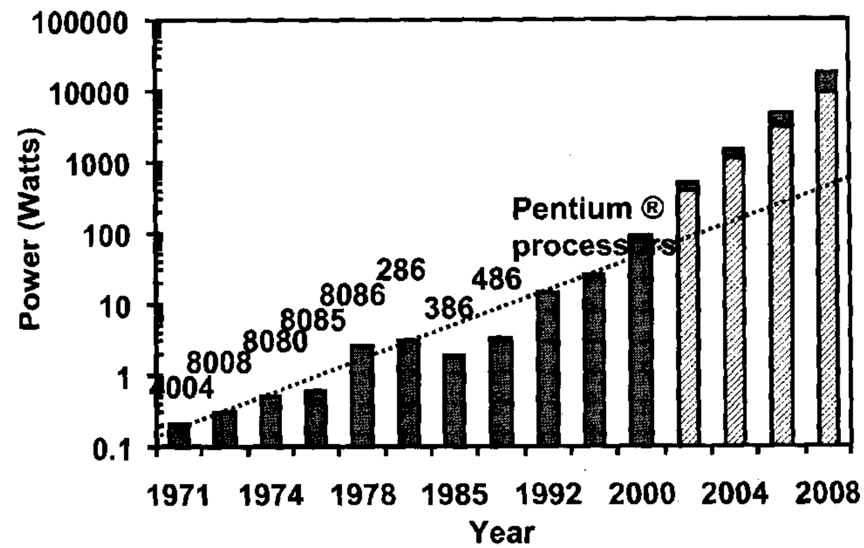


- **Advanced component technology + advanced system design**
- **Beyond CMOS + advanced More than Moore integration with More Moore**

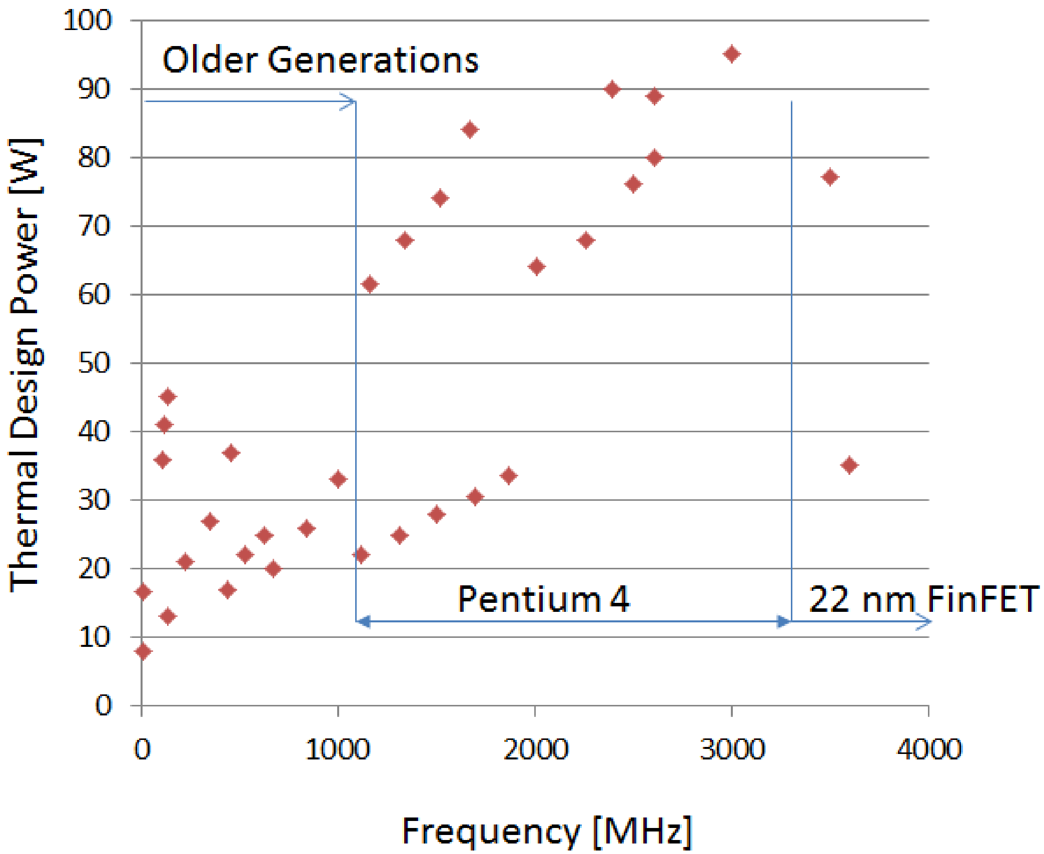
For systems 2020 and beyond

Thermal Effects and Scaling

- Intel VP Patrick Gelsinger (ISSCC 2001)
  - If scaling continues at present pace, by 2005, high speed processors would have power density of nuclear reactor, by 2010, a rocket nozzle, and by 2015, surface of sun.
  - "Business as usual will not work in the future."
- Intel stock dropped 8% on the next day
- But attention to power is increasing



Thermal Design Power



- The **thermal design power (TDP)**, sometimes called **thermal design point**, refers to the maximum amount of power the cooling system in a computer is required to dissipate.
- For example, a laptop's CPU cooling system may be designed for a 20 watt TDP, which means that it can dissipate up to 20 watts of heat without exceeding the maximum junction temperature for the computer chip.

‘Church of St. Pantelejmon’, Skopje, Republic of Macedonia (12th century Byzantine church)

Thermal Effects

Electro-Thermal Effects

Thermo-Electric Effects

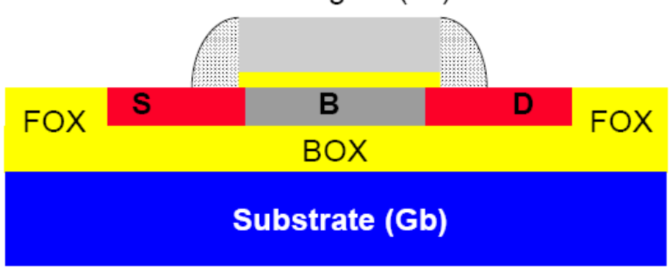
Analogy Between Electrical and Thermal Variables

Electro-Thermal Effects

- Joule Heating:
  - When an electric current flows through a solid or liquid with finite conductivity, electric energy is converted to heat through resistive losses in the material.
  - The heat is generated on the microscale when the conduction electrons transfer energy to the conductors atoms through collisions.
  - Joule heating is in some cases unwanted, and efforts are made to reduce it.
    - However, many applications rely on Joule heating;
      - some of these use the effect directly, such as cooking plates,
      - while other applications, such as microvalves for fluid control, use the effect indirectly through thermal expansion.

Why Electro-Thermal Effects in Devices?

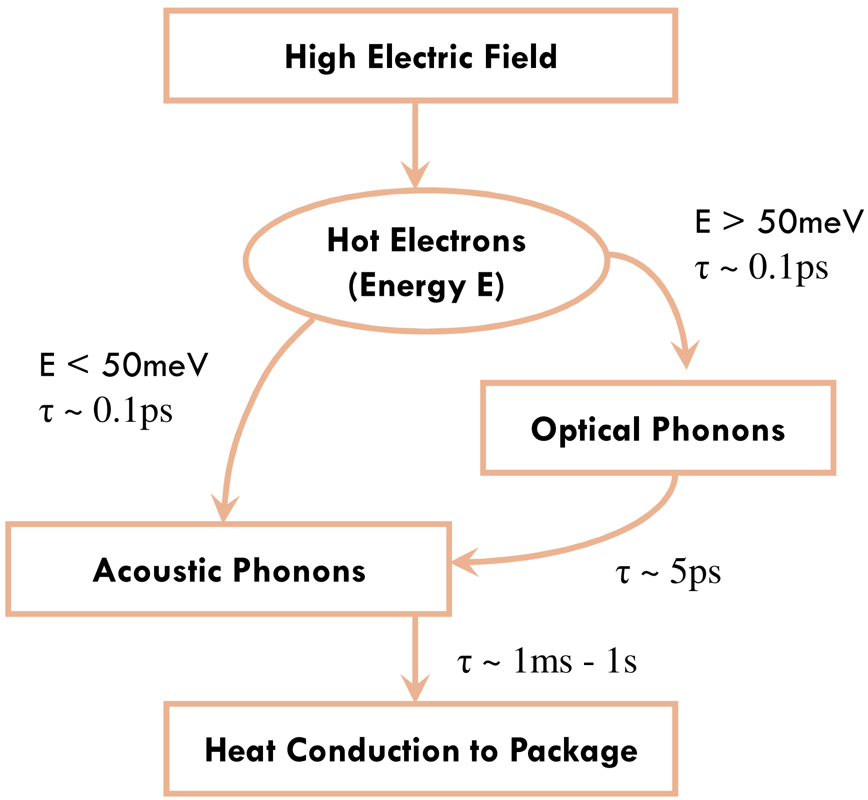
Reason for Observation of Self-Heating



Fully depleted (FD) body

Material	k_{th} (W/mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO_2	1.4

MUSTs in the Theoretical Model



E. Pop, R.W Dutton, K.E. Goodson, "Analytic Band Monte Carlo Model for Electron Transport in Si Including Acoustic and Optical Phonon Dispersion," *J. Appl. Phys.* **96**, 4998 (2004)

Implementation of Electro-Thermal Effects in Commercial Simulators

- Silvaco ATLAS implements **Wachutka** model for lattice heating which accounts for:
  - Joule heating
  - Cooling due to carrier generation and recombination
  - Peltier and Thomson effects

$$C\frac{\partial T_L}{\partial t} = \nabla \bullet \left(\kappa \nabla T_L \right) + H$$

Heat capacitance per unit volume

Thermal conductivity

Heat generation

Wachutka, G.K., "Rigorous Thermodynamic Treatment of Heat Generation in Semiconductor Device Modeling", *IEEE Trans., Computer-Aided Design* Vol. 9, No. 11 (1990): 1141-1149.

Heat Generation Model

- In the past, the heat generation model was simply:

$$H = (J_n + J_p) \bullet E$$

- Presently:

$$H = \frac{|J_n|^2}{q\mu_n n} + \frac{|J_p|^2}{q\mu_p p} -$$ → Joule heating term

$$-T_L\left(J_n \nabla P_n\right) - T_L\left(J_p \nabla P_p\right) +$$ → Peltier and Joule-Thomson effects

$$+q(R-G)\left[T_L\left(\frac{\partial \phi_n}{\partial T_{n,p}}\right) - \phi_n - T_L\left(\frac{\partial \phi_p}{\partial T_{n,p}}\right) + \phi_p\right] -$$

$$-T_L\left[\left(\frac{\partial \phi_n}{\partial T_{n,p}}\right) + P_n\right]\nabla \bullet J_n - T_L\left[\left(\frac{\partial \phi_p}{\partial T_{n,p}}\right) + P_p\right]\nabla \bullet J_p$$

→ Recombination and Generation heating and cooling terms

Wachutka, G.K., "Rigorous Thermodynamic Treatment of Heat Generation in Semiconductor Device Modeling", *IEEE Trans., Computer-Aided Design* Vol. 9, No. 11 (1990): 1141-1149.

Non-Isothermal Current Densities

- When SILVACO GIGA module is being invoked, the electron and hole current densities are modified to account for spatially varying lattice temperatures:

$$J_n = -q\mu_n n\left(\nabla\phi_n + P_n \nabla T_L\right)$$

$$J_p = -q\mu_p p\left(\nabla\phi_p + P_p \nabla T_L\right)$$

- Where P_n and P_p are absolute thermoelectric powers for electrons and holes and are calculated using:

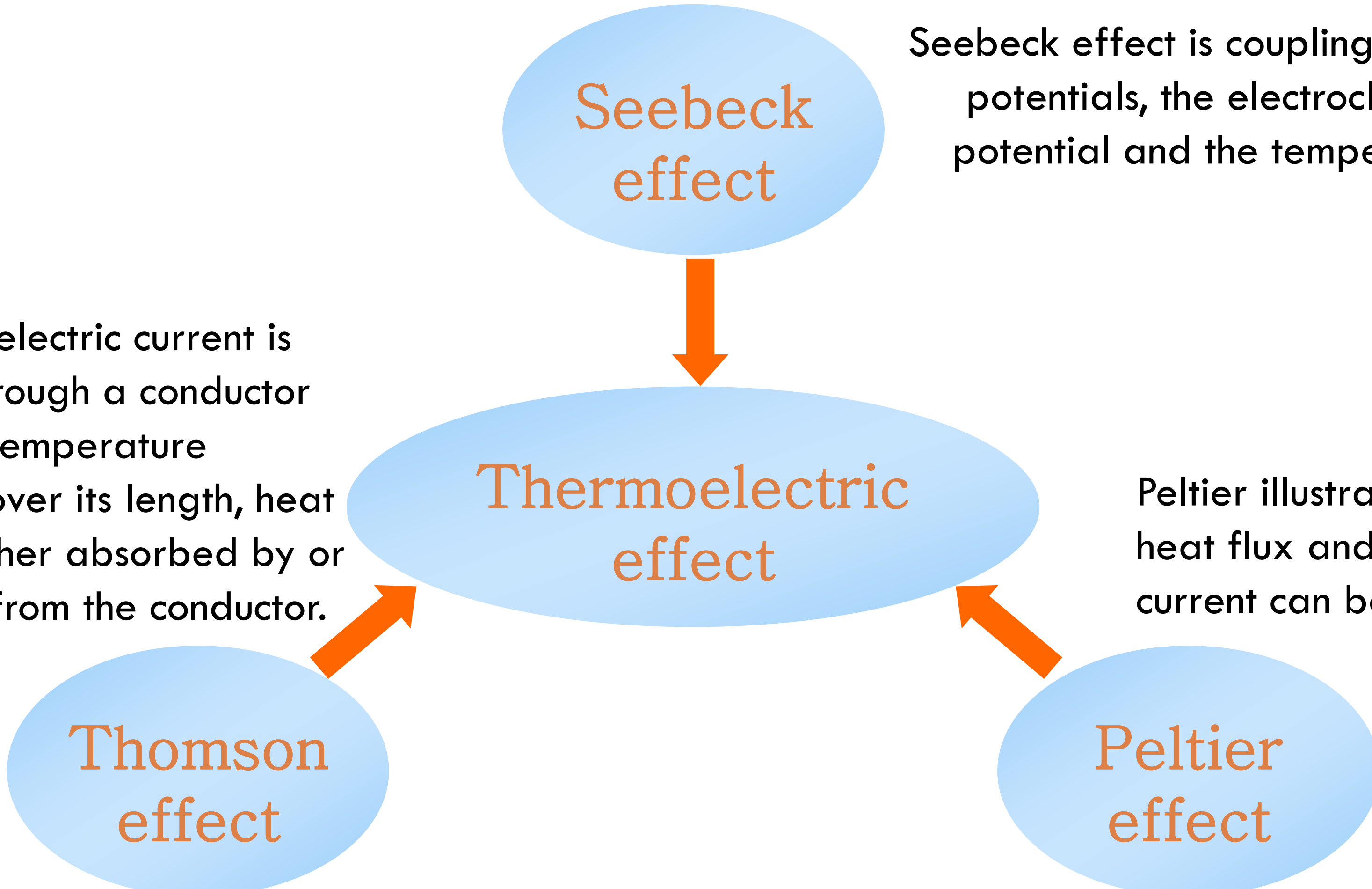
$$P_n = -\frac{k_B}{Q}\left(\frac{5}{2} + \ln\left(\frac{N_c}{n}\right) + KSN + \zeta_n\right)$$

$$P_p = \frac{k_B}{Q}\left(\frac{5}{2} + \ln\left(\frac{N_v}{p}\right) + KSP + \zeta_p\right)$$

Wachutka, G.K., "Rigorous Thermodynamic Treatment of Heat Generation in Semiconductor Device Modeling", *IEEE Trans., Computer-Aided Design* Vol. 9, No. 11 (1990): 1141-1149.

Thermo-Electric Effects

Seebeck effect is coupling of two potentials, the electrochemical potential and the temperature.



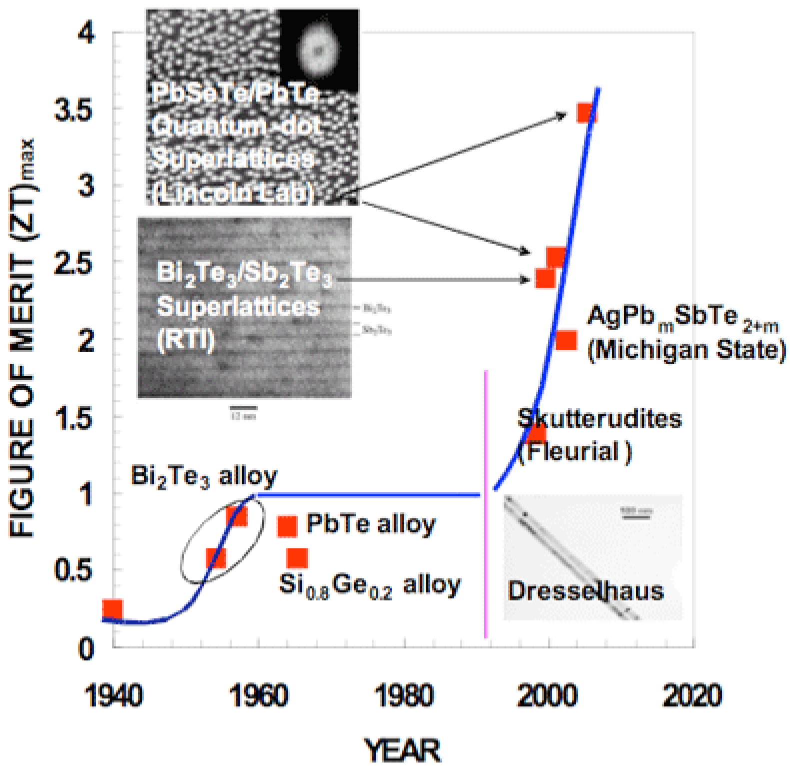
When an electric current is passed through a conductor having a temperature gradient over its length, heat will be either absorbed by or expelled from the conductor.

Peltier illustrated that heat flux and electrical current can be coupled.

Thermo-Electric Effects

- When any two metals are connected together, a voltage is developed which is a function of the temperatures of the junctions and (mainly) the difference in temperatures.
- It was later found that the Seebeck voltage is the sum of two effects: the ***Peltier effect***, and the ***Thompson effect***.
  - The ***Peltier effect*** explains a voltage generated in a junction of two metal wires.
  - The ***Thompson effect*** explains a voltage generated by the temperature gradient in the wires.

Peltier Effect: ZT Factor Over the Years



$$ZT = S^2T\,\sigma/\kappa$$

- The ZT of a thermoelectric material is a dimensionless unit that is used to compare the efficiencies of various materials.
- ZT is determined by three physical parameters:
  - the thermopower S (also known as Seebeck factor),
  - the electrical conductivity σ, the thermal conductivity $k = k_e + k_{ph}$, where the k_e and k_{ph} are the thermal conductivities of electrons and phonons, respectively,
  - and the absolute temperature T

Analogy Between Electrical and Thermal Variables

$$J = \sigma E = -\sigma \frac{dV}{dx} \therefore current\ density$$

$$F = -\kappa \frac{dT}{dx} \therefore heat\ flux$$

$$\begin{cases} J \Leftrightarrow F \\ V \Leftrightarrow T \\ \sigma \Leftrightarrow \kappa \end{cases}$$

Previous Work Done in Thermal Modeling

Previous Work in Thermal Modeling

- Mostly, the previous work performed and related to thermal modeling can be split into:
  - Solutions of the Phonon Boltzmann Transport Equation
  - Analysis of self-heating effects in devices

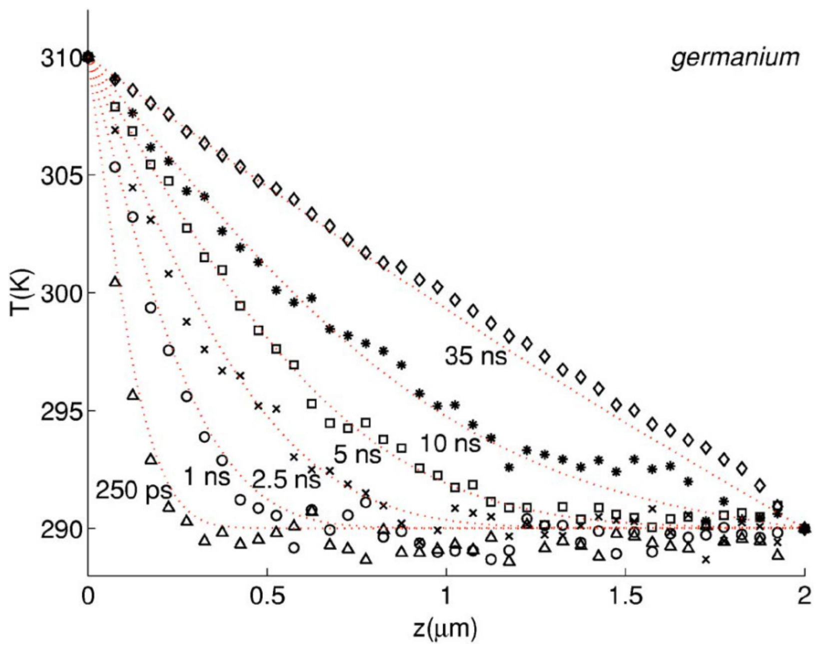
Phonon BTE Solvers

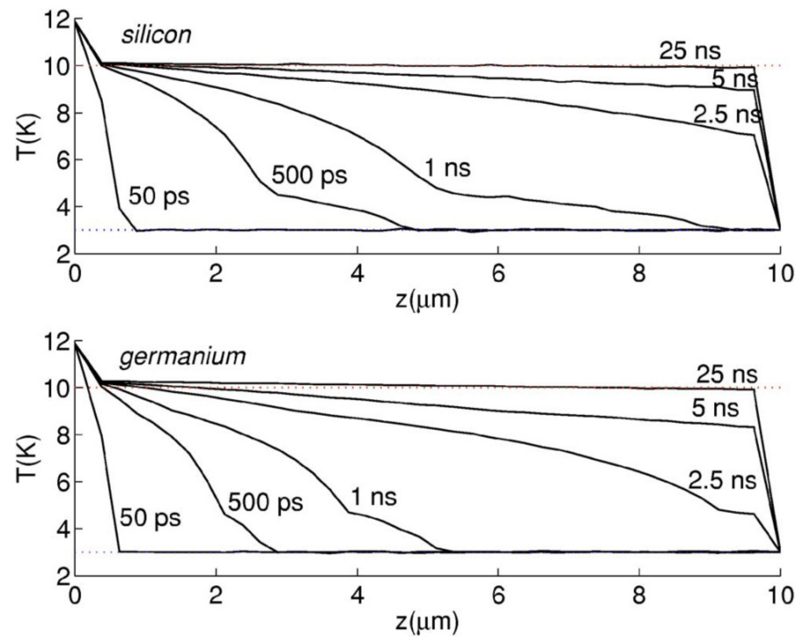
- ***Peterson*** performed a Monte Carlo Simulation for phonons in the Debye approximation and using single relaxation time
- ***Mazumder and Majumdar*** followed Peterson approach but included the dispersion relation and the different acoustic polarization branches
  - Limit: The N and the U processes are not treated separately although they do not contribute the same way to the thermal conductivity

* Peterson, R. B. (1994). "Direct Simulation of Phonon-Mediated Heat Transfer in a Debye Crystal." *Journal of Heat Transfer*, Vol. 116(4), pp. 815-822.
* Mazumder, S. and Majumdar, A. (2001). "Monte Carlo Study of Phonon Transport in Solid Thin Films Including Dispersion and Polarization." *Journal of Heat Transfer*, Vol.123(4), pp. 749-759.

Phonon BTE Solvers, Cont'd

- ***Lacroix*** further generalized the model:
  - By incorporation of N and U processes
  - Transient conditions are also being considered





Lacroix, D., Joulain, K. and Lemonnier, D. (2005). "Monte Carlo Transient Phonon Transport in Silicon and Germanium at Nanoscales." *Physical Review B*, Vol. 72(6), pp. 064305/1-11.

Modeling Self-Heating in Devices

- Work of ***Eric Pop, Goodson, Robert Dutton***
  - Non-parabolic model with analytical phonon dispersion
  - study heat transfer and energy conversion processes at nanoscales. Applications include semiconductor devices and packaging, thermoelectric and photonic energy conversion, and microfluidic heat exchangers.
- Work of ***Kelsall and Sadi***
  - Nanoscale transistors, GaN HEMTs

    (next presentation)

E. Pop, R.W Dutton, K.E. Goodson, "Analytic Band Monte Carlo Model for Electron Transport in Si Including Acoustic and Optical Phonon Dispersion," *J. Appl. Phys.* **96**, 4998 (2004)

The ASU Model to Addressing Self-Heating

Theoretical Model

Application of the Model to Modeling of:

- FD SOI Devices, Dual Gate Structures, SOD and SOAlN Devices
- Nanowire Transistors
- GaN HEMTs

Theoretical Model

$$\left(\frac{\partial}{\partial t}+v_e(\mathrm{k})\cdot\nabla_r+\frac{e}{\hbar}E(\mathrm{r})\cdot\nabla_k\right)f=\sum_{\mathrm{q}}\left\{W_{e,\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}+W_{a,-\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}-W_{e,-\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}-W_{a,\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}\right\}$$

$$\left(\frac{\partial}{\partial t}+v_p(q)\cdot\nabla_r\right)g=\sum_{\mathrm{k}}\left\{W_{e,\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}-W_{a,\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}\right\}+\left(\frac{\partial g}{\partial t}\right)_{p-p}$$

J. Lai and A. Majumdar, “Concurent thermal and electrical modeling of submicrometer silicon devices”, J. Appl. Phys. , Vol. 79, 7353 (1996).

$$C_{LO}\frac{\partial T_{LO}}{\partial t}=\frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-LO}}\right)+\frac{nm^*v_d^2}{2\tau_{e-LO}}-C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right),$$

$$C_A\frac{\partial T_A}{\partial t}=\nabla\cdot\left(k_A\nabla T_A\right)+C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right)+\frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-L}}\right).$$

K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Theoretical Model …

Energy gain from the electrons

Energy loss to acoustic phonons

$$C_{LO}\frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2}\left(\frac{T_e - T_L}{\tau_{e-LO}}\right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right),$$

$$C_A\frac{\partial T_A}{\partial t} = \nabla\cdot\left(k_A \nabla T_A\right) + C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) + \frac{3nk_B}{2}\left(\frac{T_e - T_L}{\tau_{e-L}}\right).$$

Heat Diffusion

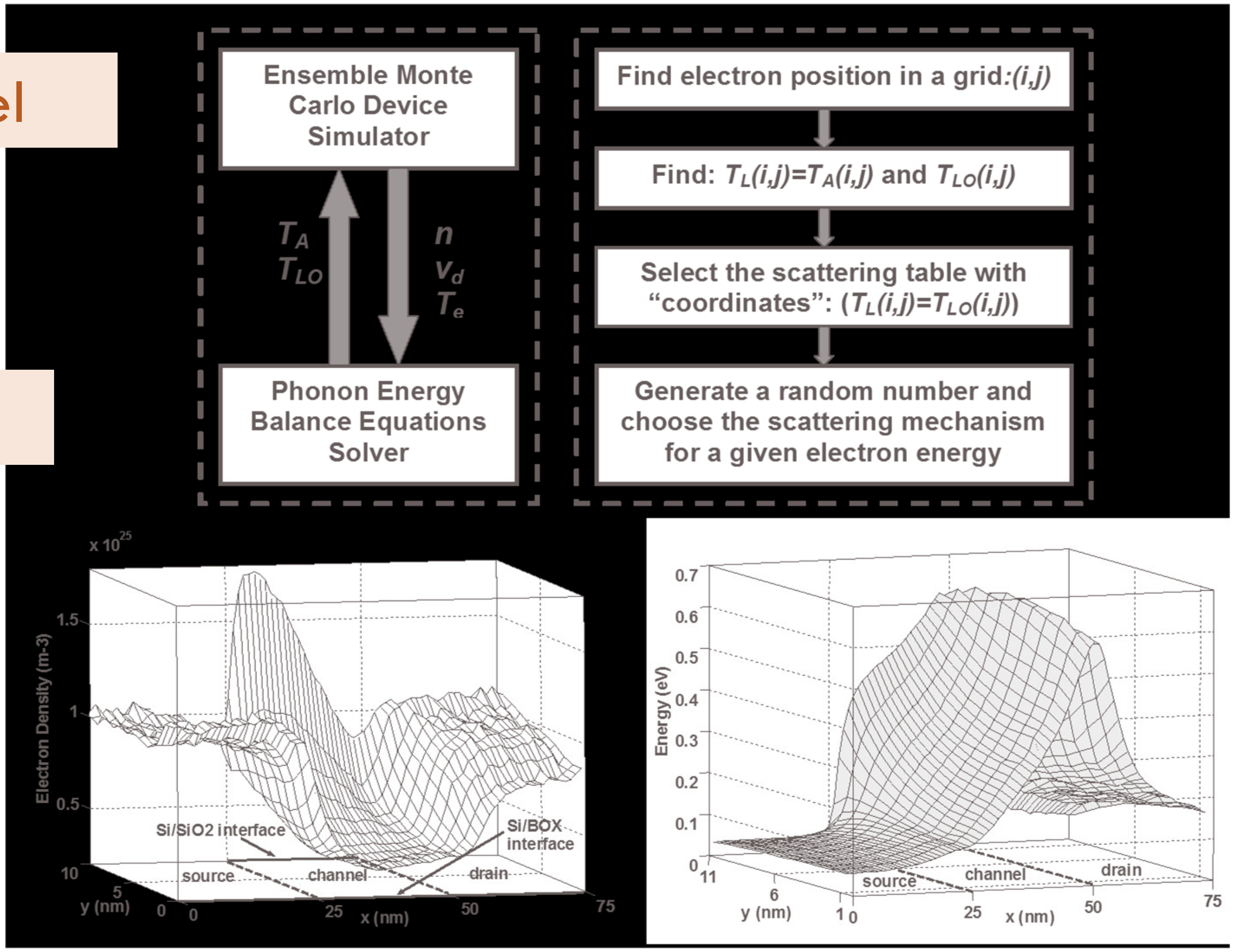
Gain term due to optical phonons

Gain term due to electrons (omitted if acoustic phonon scattering is treated as elastic scattering process)

Theoretical Model …

Particle Model

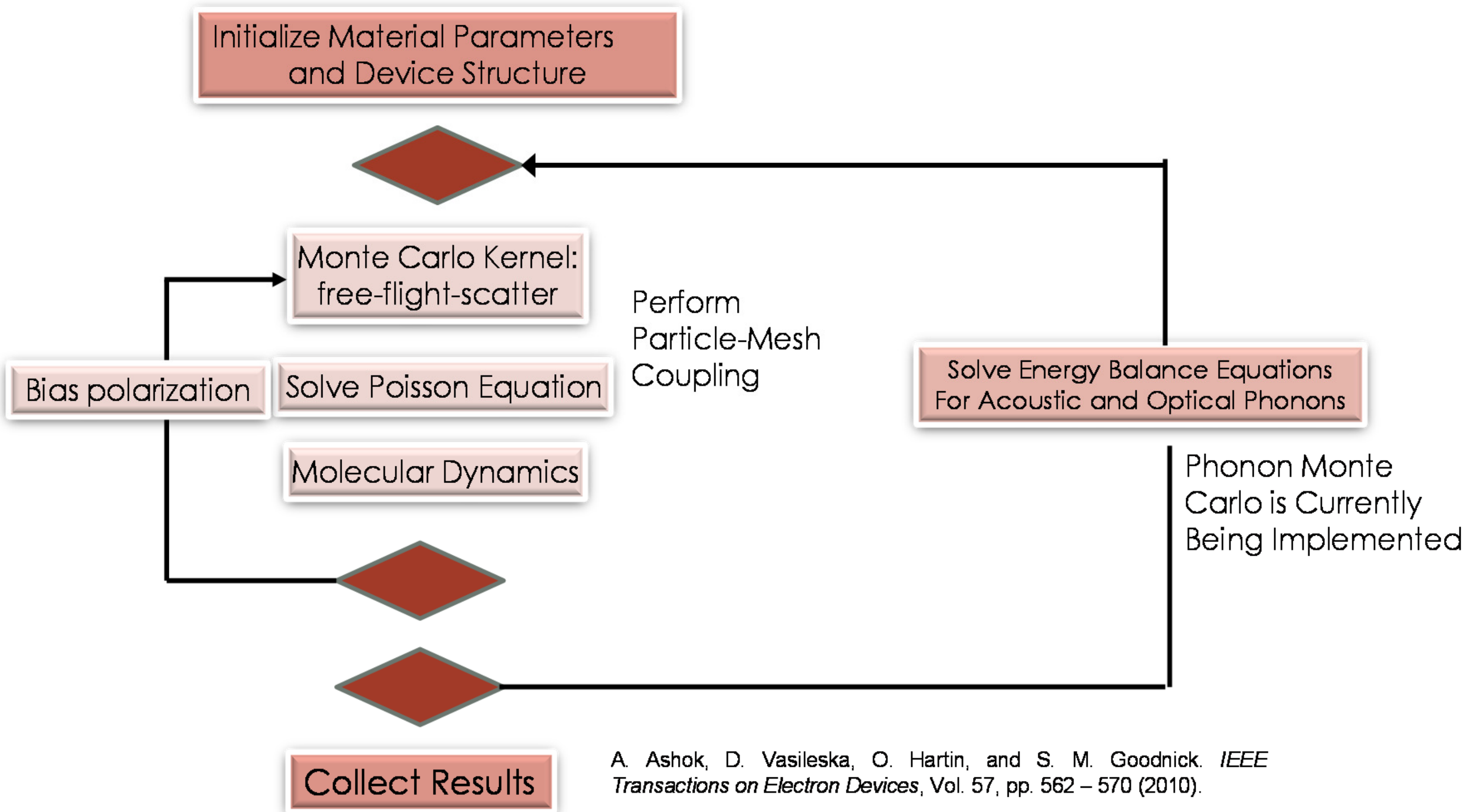
Fluid Model



K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Theoretical Model ...

- Gummel cycles



A. Ashok, D. Vasileska, O. Hartin, and S. M. Goodnick. *IEEE Transactions on Electron Devices*, Vol. 57, pp. 562 – 570 (2010).

K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Theoretical Model: Thermal Conductivity

- Solid transmit thermal energy by two modes , either one of which, or both, may operate.

  1. In all solids , energy may be transferred by means of elastic vibrations of the lattice moving through the crystal in the form of waves .
  2. In some solids , notably metals , free electrons moving through the lattice also carry energy in a manner similar to thermal conduction by a True gas phase .

Thermal Conductivity: $k = k_e + k_p$

Thermal Conductivity

$$k_p = \frac{1}{3} C\ v\ l$$

Specific heat (C), Sound velocity (v), Phonon *mfp* (l)

Specific heat :

If $T > \Theta$, $C \sim constant$

If $T << \Theta$, $C \sim T^d$ (d: dimension)

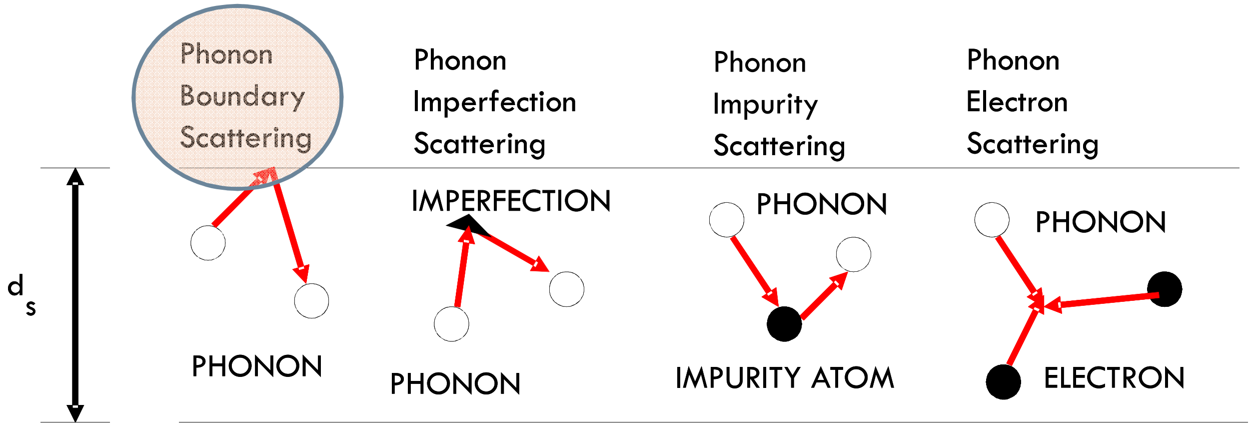
Mean free path:

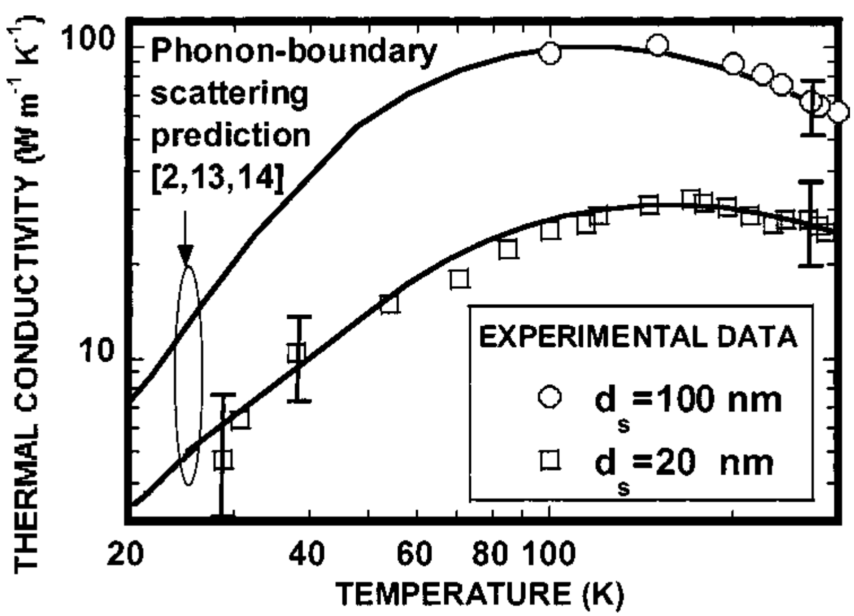
$$\frac{1}{l} = \frac{1}{l_{st}} + \frac{1}{l_{um}}$$

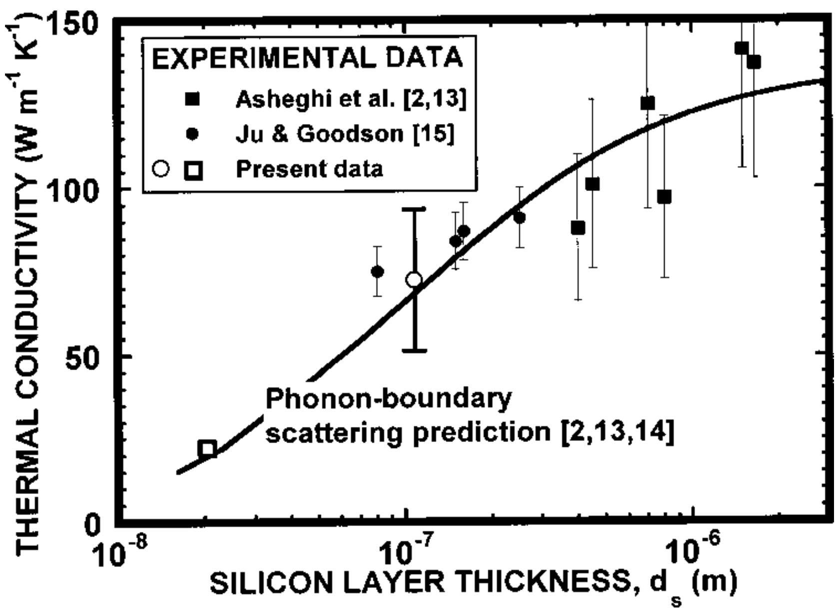
Static scattering (phonon -- defect, boundary): $l_{st} \sim constant$

Umklapp phonon scattering: $l_{um} \sim e^{\Theta/T}$

Thermal Conductivity of Thin Films





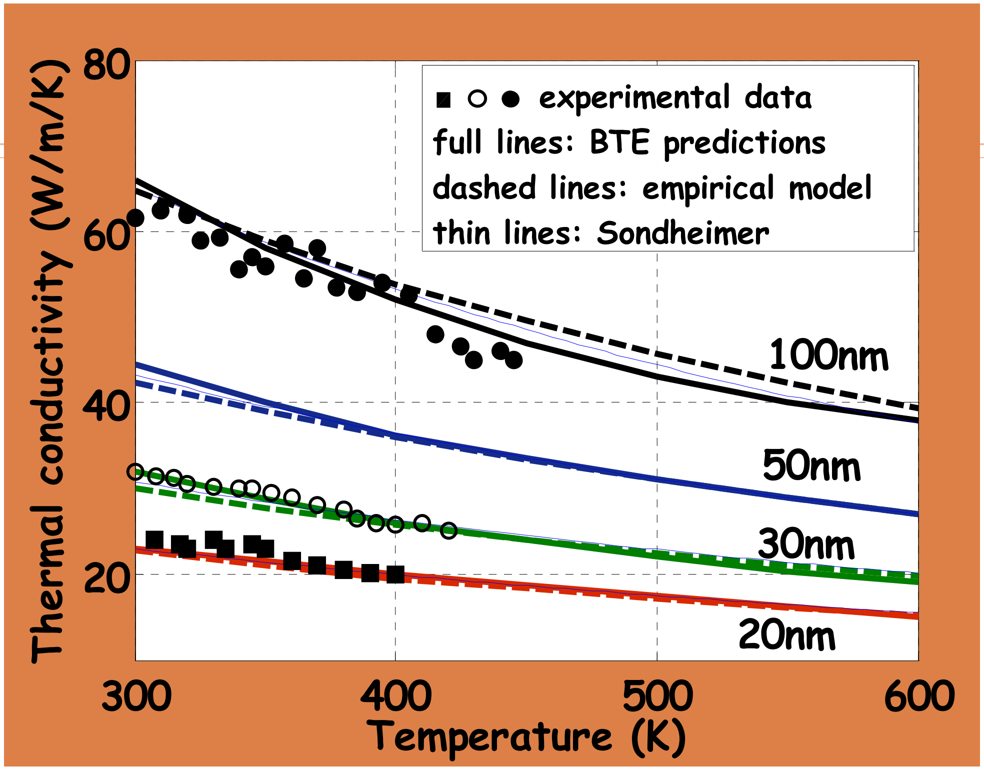


Analytical Model for Thin Films

$$\kappa(z)=\kappa_0(T)\int_0^{\pi/2}\sin^3\theta\left\{1-\exp\left(-\frac{a}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{a-2z}{2\lambda(T)\cos\theta}\right)\right\}d\theta$$

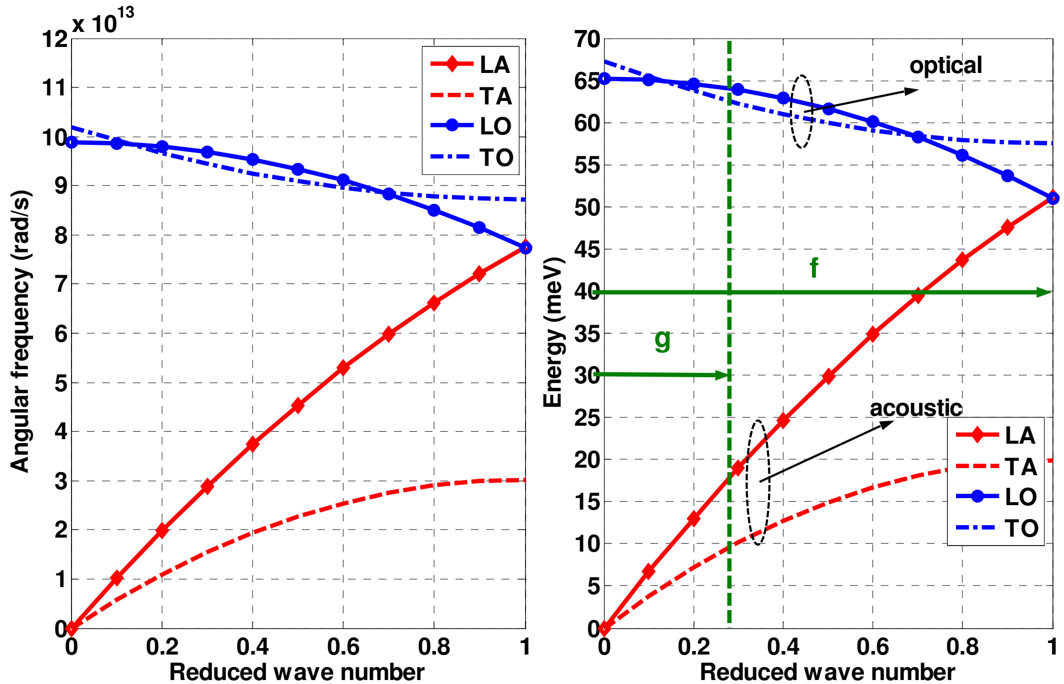
$$\lambda(T)=\lambda_0(300/T)$$

$$\kappa_0(T)=\frac{135}{a+bT+cT^2}\quad \text{W/m/K}$$



- E. H. Sondheimer, "The Mean Free Path of Electrons in Metals", Advances in Physics, Vol. 1, no. 1, Jan. 1952, reprinted in Advances in Physics, Vol. 50, pp. 499-537, 2001.
- M. Asheghi,., M. N. Touzelbaev., K. E. Goodson, Y. K. Leung, and S. S. Wong., "Temperature Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," ASME Journal of Heat Transfer, Vol.120, pp. 30-33, 1998.

Theoretical Model – Phonon Dispersions



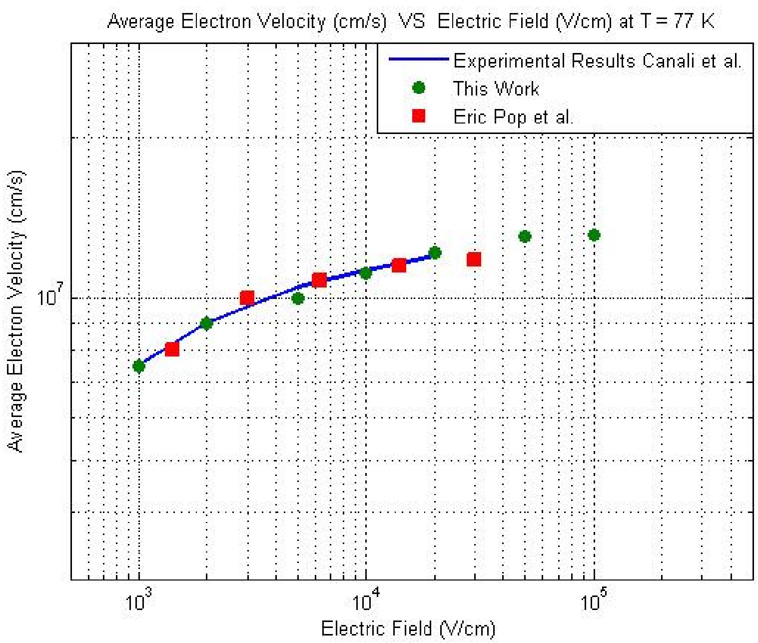
QUADRATIC FIT TO PHONON DISPERSIONS

	ω_o (10^{13} rad/s)	υ_s (10^5 cm/s)	c 10^{-3} cm^2/s
LA	0.00	9.01	-2.00
TA	0.00	5.23	-2.26
LO	9.88	0.00	-1.60
TO	10.20	-2.57	1.11

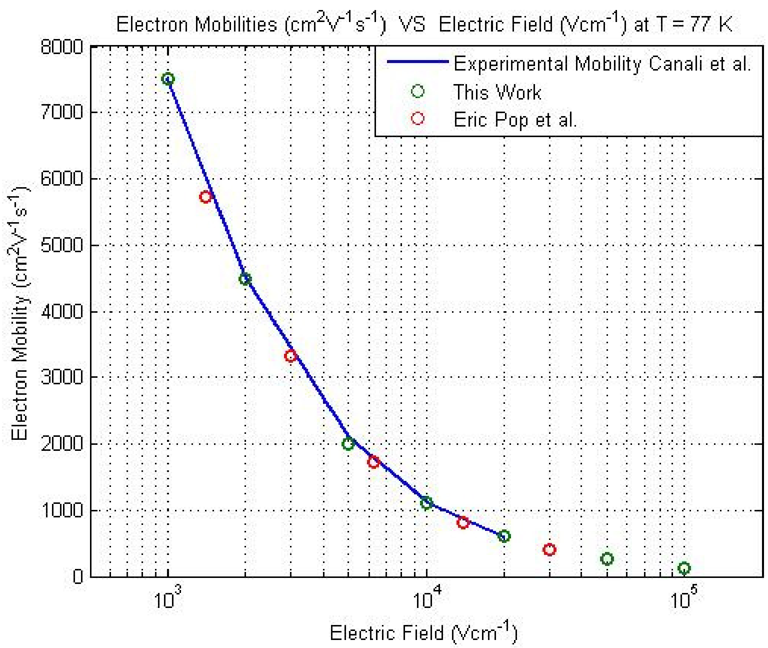
E. Pop, R.W Dutton, K.E. Goodson, "Analytic Band Monte Carlo Model for Electron Transport in Si Including Acoustic and Optical Phonon Dispersion," *J. Appl. Phys.* **96**, 4998 (2004)

Phonon Dispersions: Proof of Concept

Drift Velocity in Silicon at T=77K

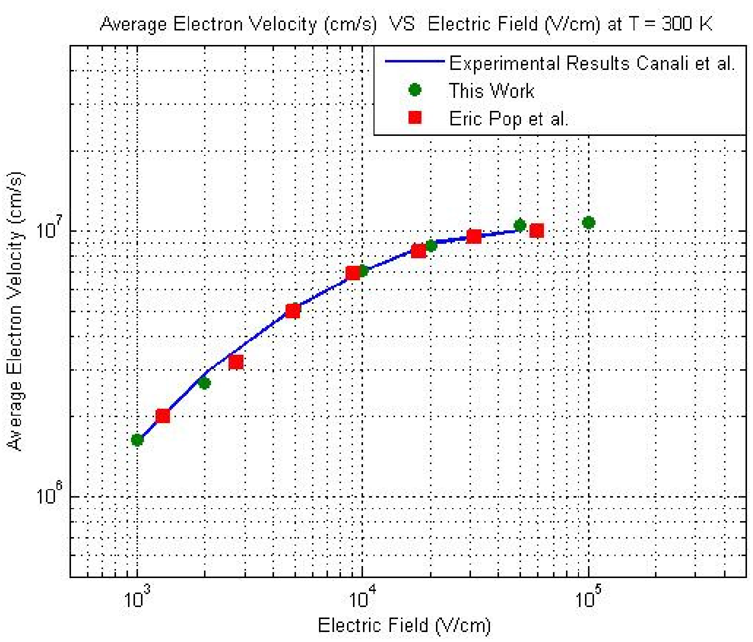


Mobility at T=77K

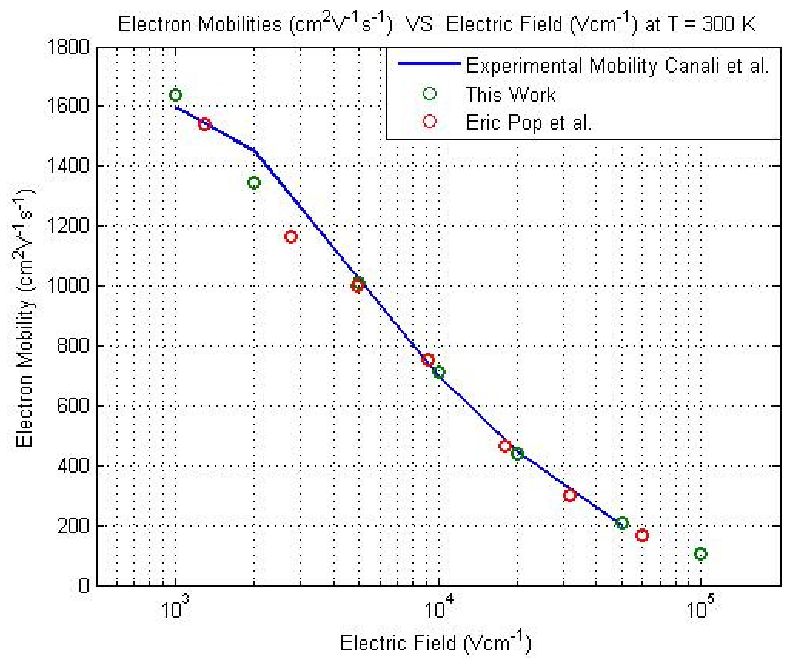


Phonon Dispersions: Proof of Concept

Drift Velocity in Silicon at T=300K



Mobility at T=300K

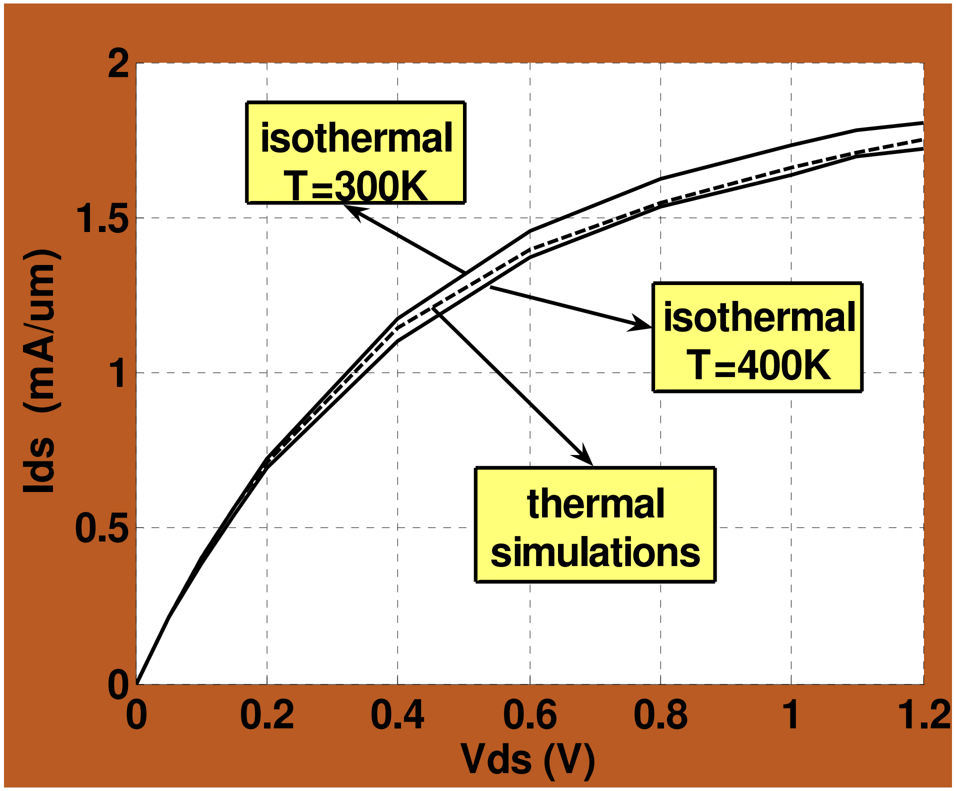


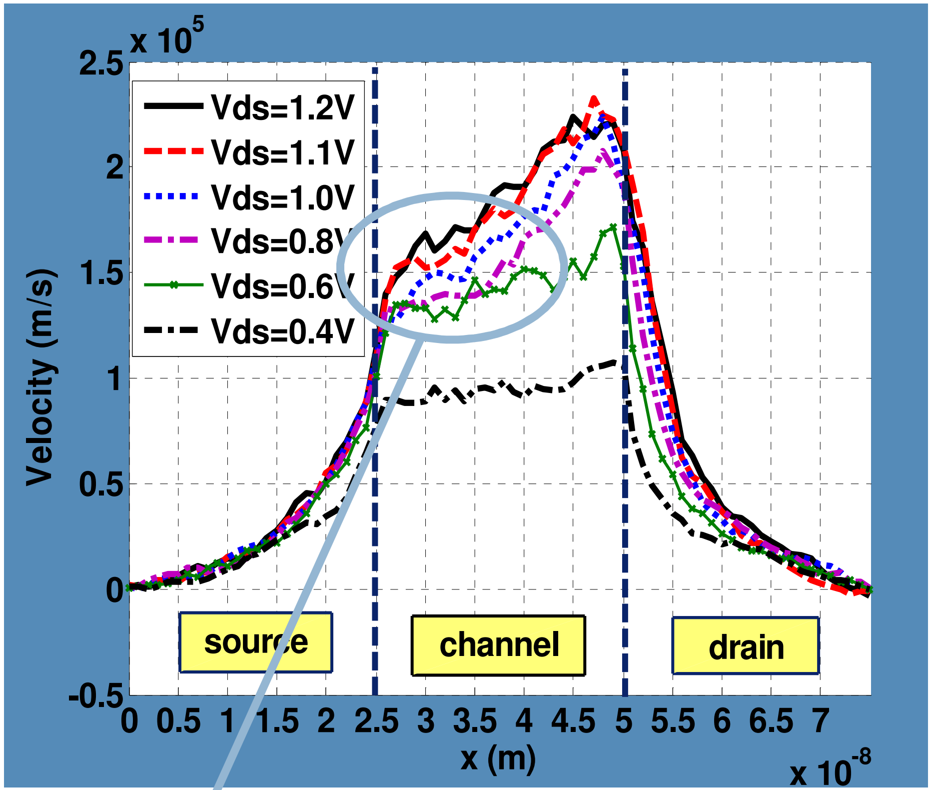
FULLY DEPLETED SOI DEVICES

Lake Powell, Arizona

Simulation Results: FD SOI Devices

- 25 nm Channel Length Device

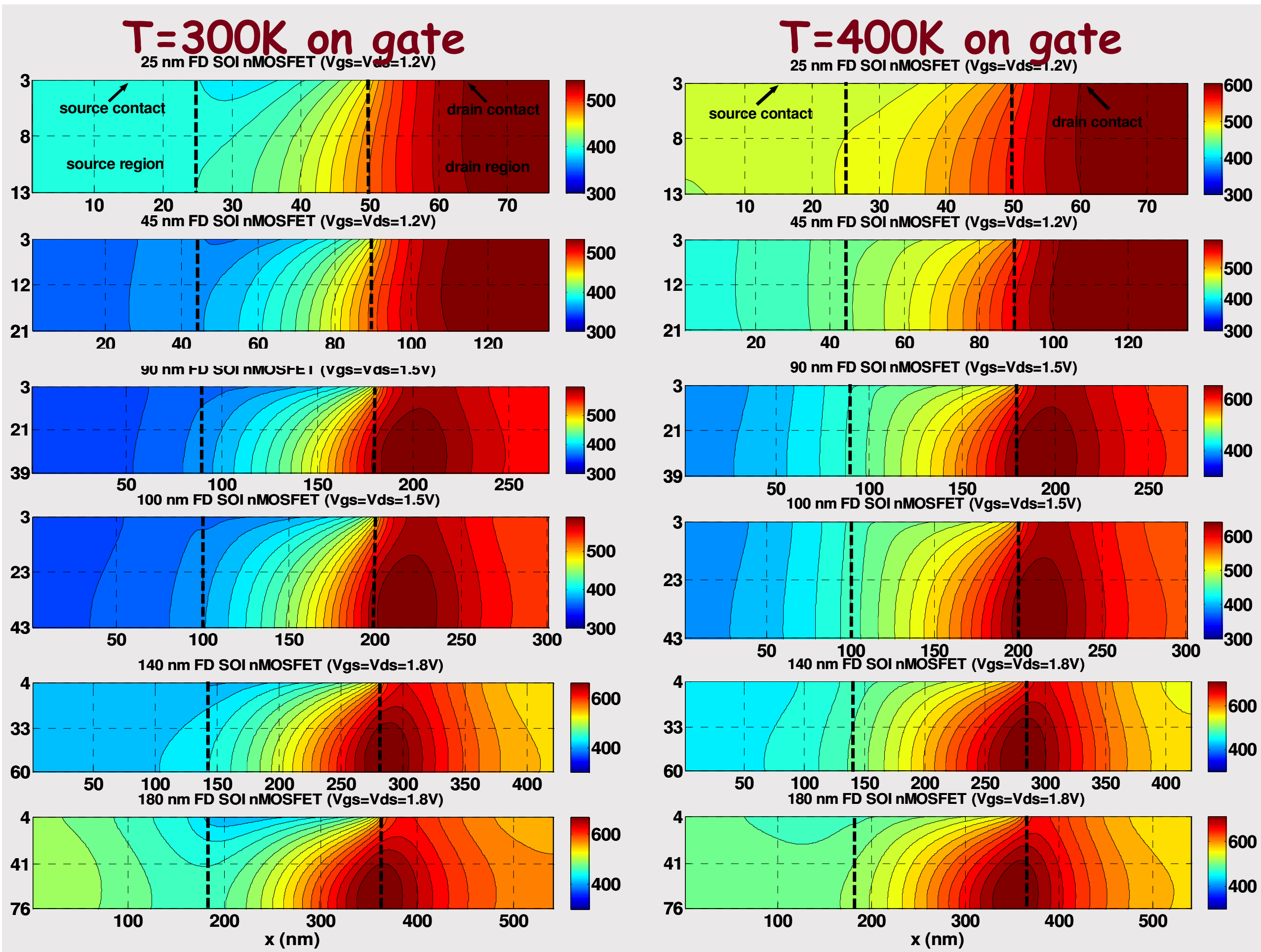




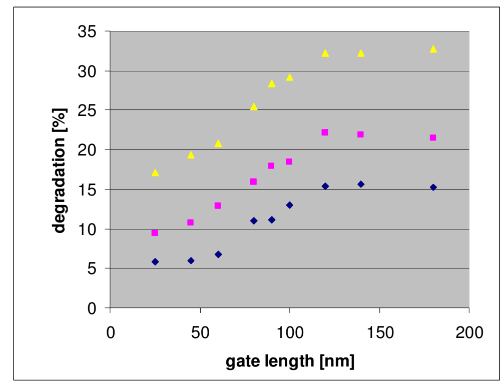
K. Raleva, D. Vasileska, S. M. Goodnick and T. Dzekov, "Modeling thermal effects in nano-devices", *Journal of Computational Electronics, DOI 10.1007/s10825-008-0189-3 © Springer Science+Business Media LLC 2008, J. Computational Electronics*, Vol. 7, pp. 226-230 (2008).

Carriers are in the velocity overshoot

Heat Dissipation Across Technology Nodes



Parameter is the temperature on the Gate Electrode.

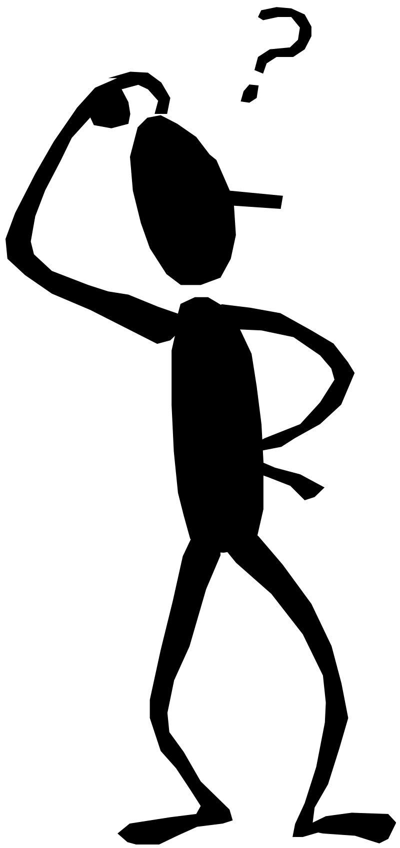


Neumann Boundary Conditions are imposed at the Artificial Boundaries and the Source and Drain contacts

K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Can We Lower Self-Heating Effects?

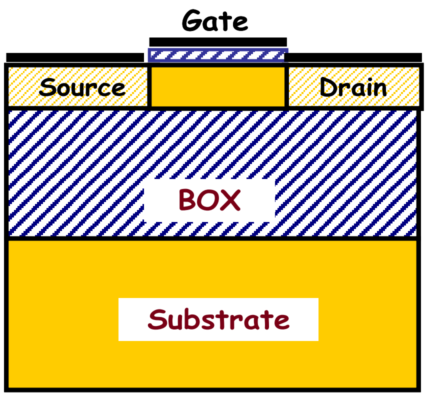
- Dual-Gate Devices
- SOI vs. SOD vs. SOAIN

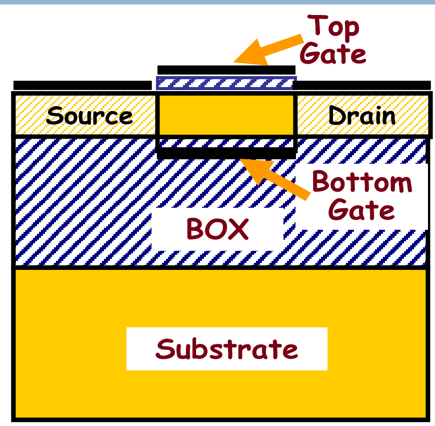


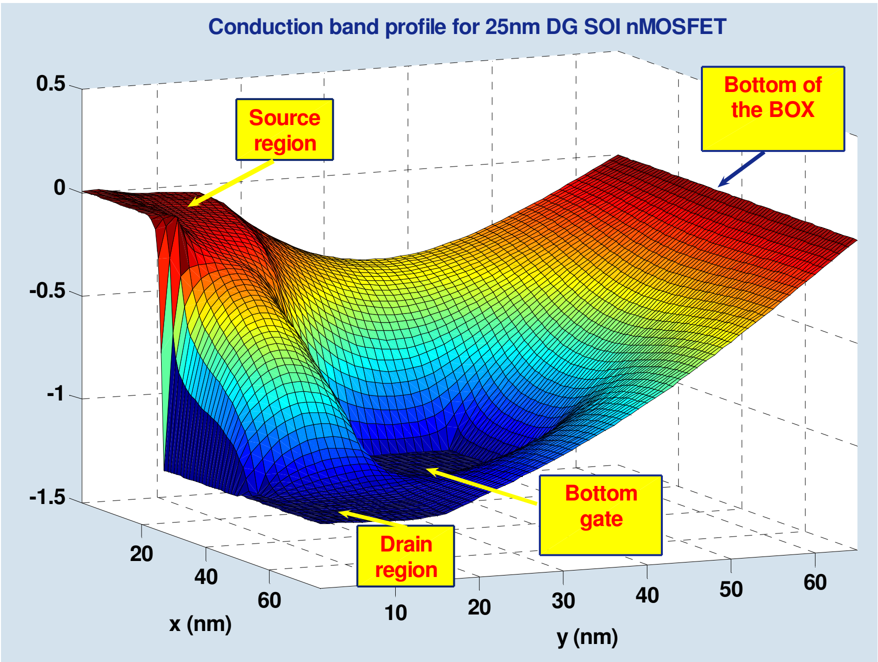
S.M. Goodnick, D. Vasileska, K. Raleva, "Is Dual Gate Device Better From a Thermal Perspective?", *Proceedings of 2008 SISPAD Conference*, pp. 125 - 128.

K. Raleva, D. Vasileska, S. M. Goodnick, Is SOD Technology the Solution to Heating Problems in SOI Devices?, Electron Device Letters, IEEE, Volume 29, Issue 6, June 2008 Page(s):621 - 624.

Dual-Gate SOI Devices



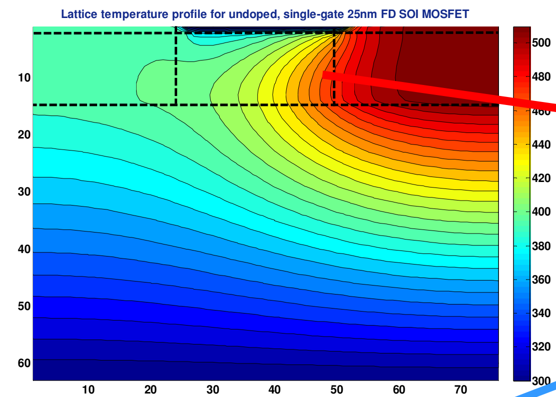


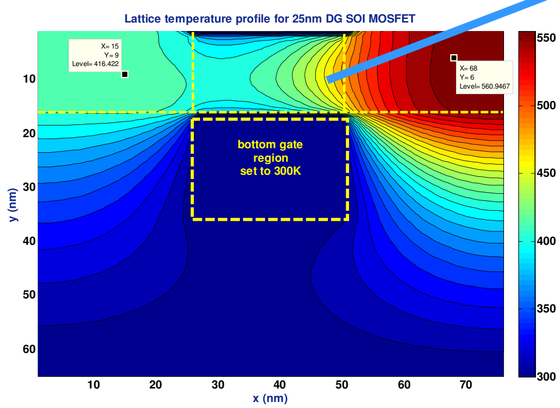


S.M. Goodnick, D. Vasileska, K. Raleva, "Is Dual Gate Device Better From a Thermal Perspective?", *Proceedings of the 2008 SISPAD Conference*, pp. 125 - 128.

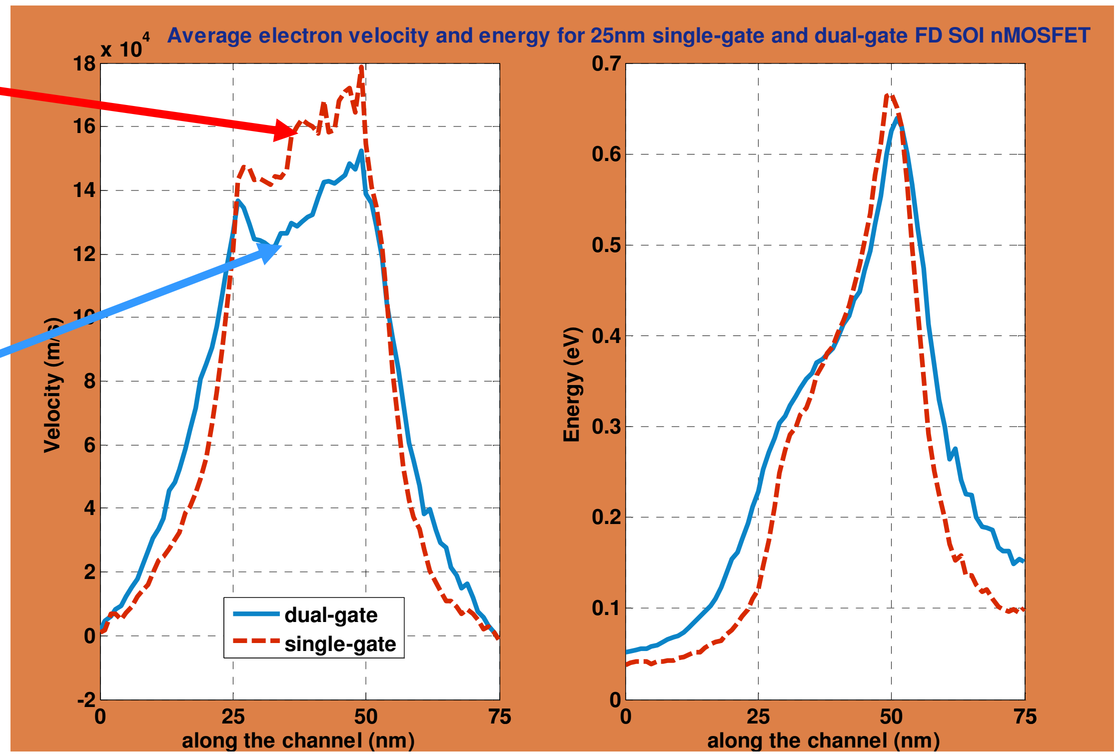
A Closer Look …

Single gate lattice temperature profile





Dual gate lattice temperature profile



Where Does the Benefit of the DG Structure Comes From?

25nm FD SOI nMOSFET

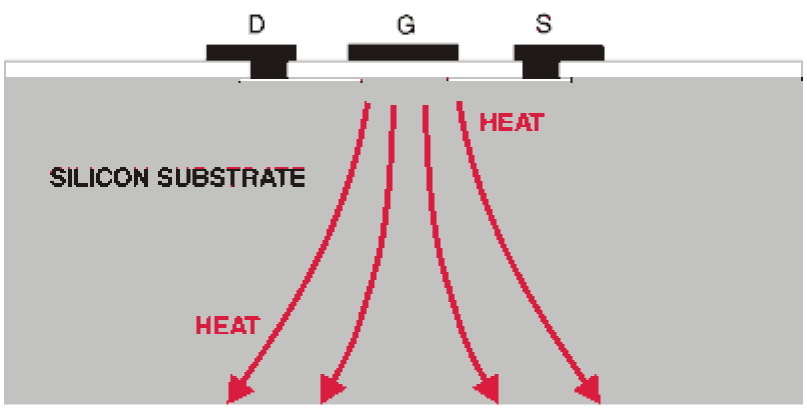
Type of simulation	*Gate temperature*	*Bottom of the BOX temperature*	*Current (mA/um)*	**Current decrease (%)**
isothermal	300K	300K	1.9428	\
thermal	300K	300K	1.7644	**9.18**
thermal	400K	300K	1.6641	**14.35**
thermal	600K	300K	1.4995	**22.82**

For almost the same Current degradation DG devices offer **1.5-1.7** times more current

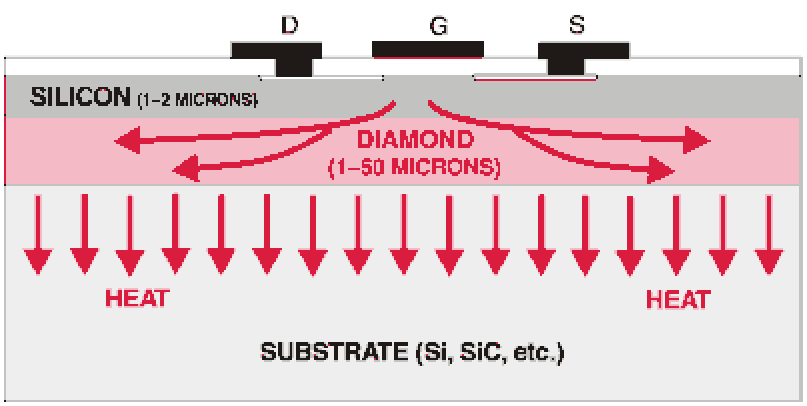
25nm DG SOI nMOSFET

25nm DG SOI nMOSFET (Vgate-top=Vgate-bottom=1.2V; Vdrain=1.2V; Vsource=0V; Vsubstrate=0V)					
Type of simulation	Top gate temperature	Bottom gate temperature	Bottom of the BOX temperature	Current (mA/um)	Current decrease (%)
isothermal	300K	300K	300K	3.0682	\
thermal	300K	300K	300K	2.7882	**9.13**
thermal	400K	400K	300K	2.6274	**14.37**
thermal	600K	600K	300K	2.3153	**24.54**

SOI vs. SOD vs. SOAlN



Standard Si technology



SOD technology

Silicon-On-Diamond and Silicon-On-Aluminum Nitride (SOAlN) Technologies as viable alternatives to Silicon-On-Insulator Devices

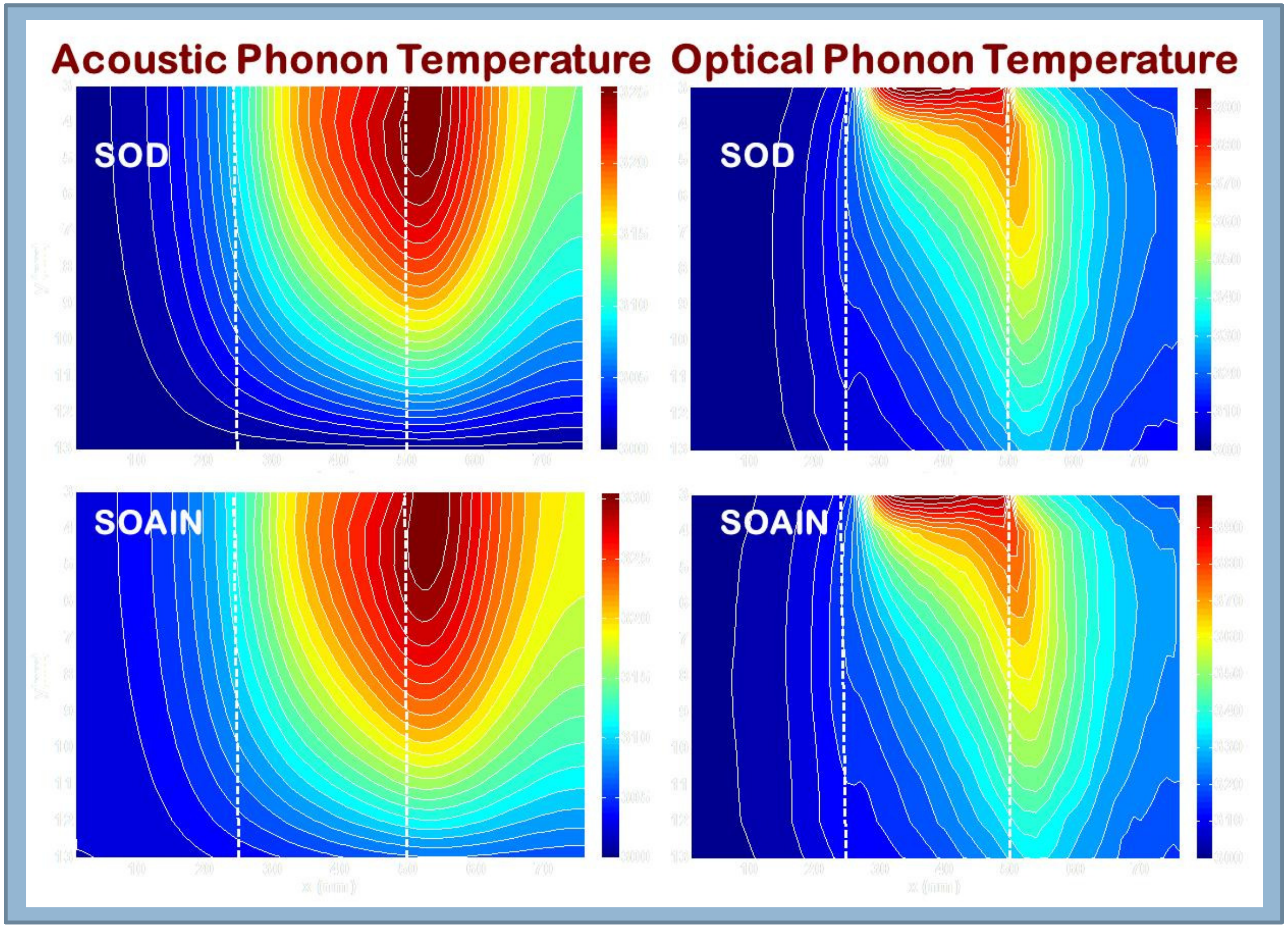
BOX Material	Dielectric constant	K_{th} (W/mK)
SiO_2	3.9	1.38
Diamond	5.68	2000
AlN	9.14	272

Current Degradation

Device	Device width=3um (without substrate)			Device width=3um (with substrate)		
	Current (mA/um) isothermal	Average Current (mA/um) thermal	Current Decrease (%)	Current (mA/um) isothermal	Average Current (mA/um) thermal	Current Decrease (%)
SOI	1.82	1.70	7.05	1.82	1.70	7.05
SOAIN	1.85	1.82	1.55	1.88	1.84	2.18
SOD	1.84	1.81	1.41	1.84	1.82	1.08

K. Raleva, D. Vasileska, S. M. Goodnick, Is SOD Technology the Solution to Heating Problems in SOI Devices?, Electron Device Letters, IEEE, Volume 29, Issue 6, June 2008 Page(s):621 - 624.

Heat Spreading

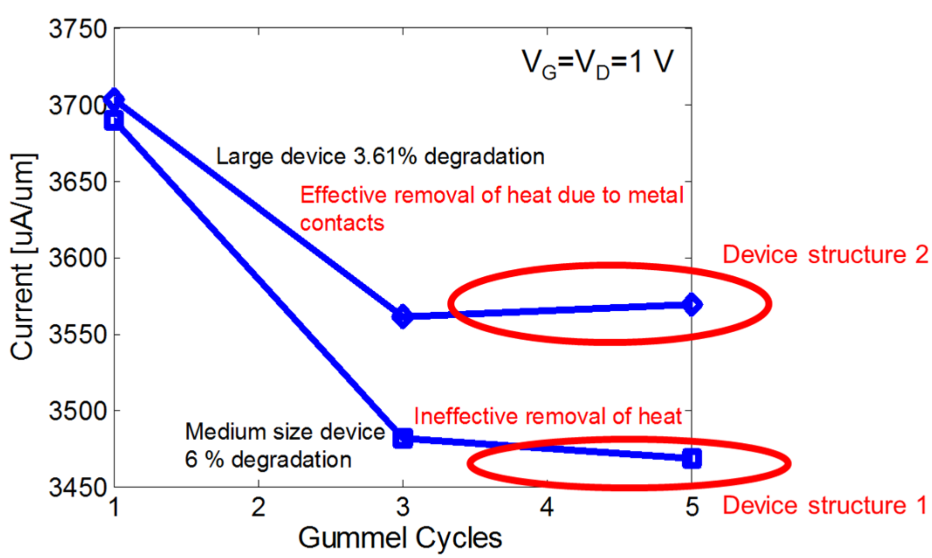


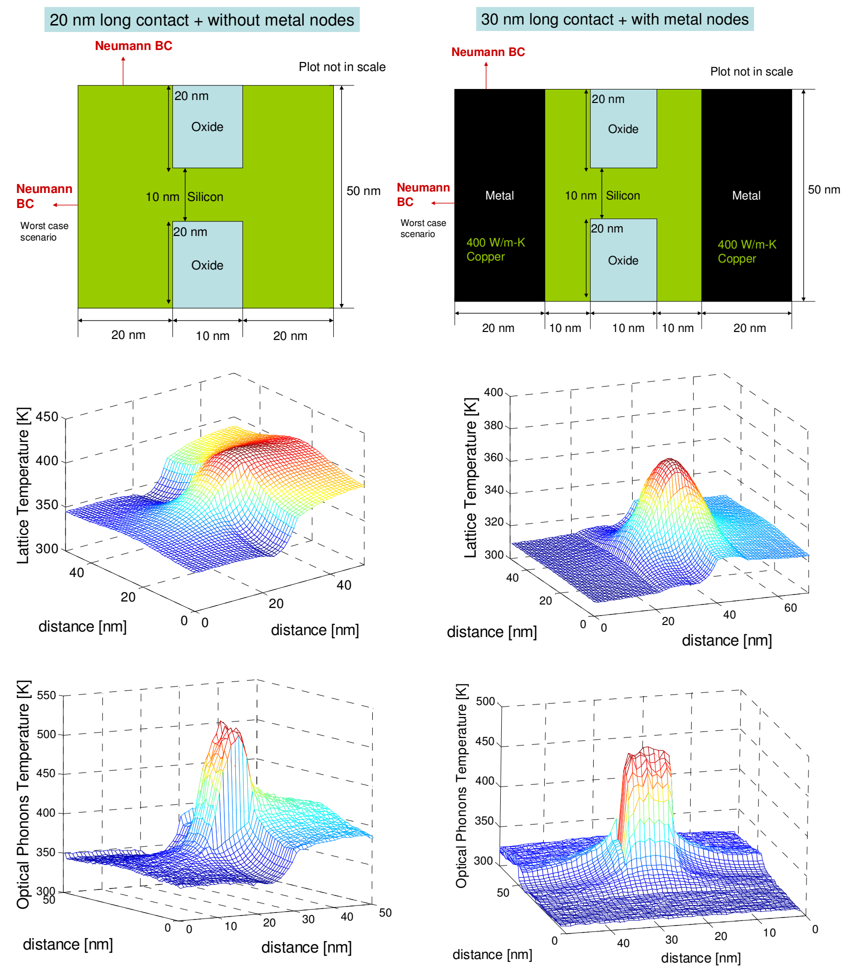
NANOWIRE TRANSISTORS

Lake Powell, Arizona

Nanowires – The Role of the Contacts

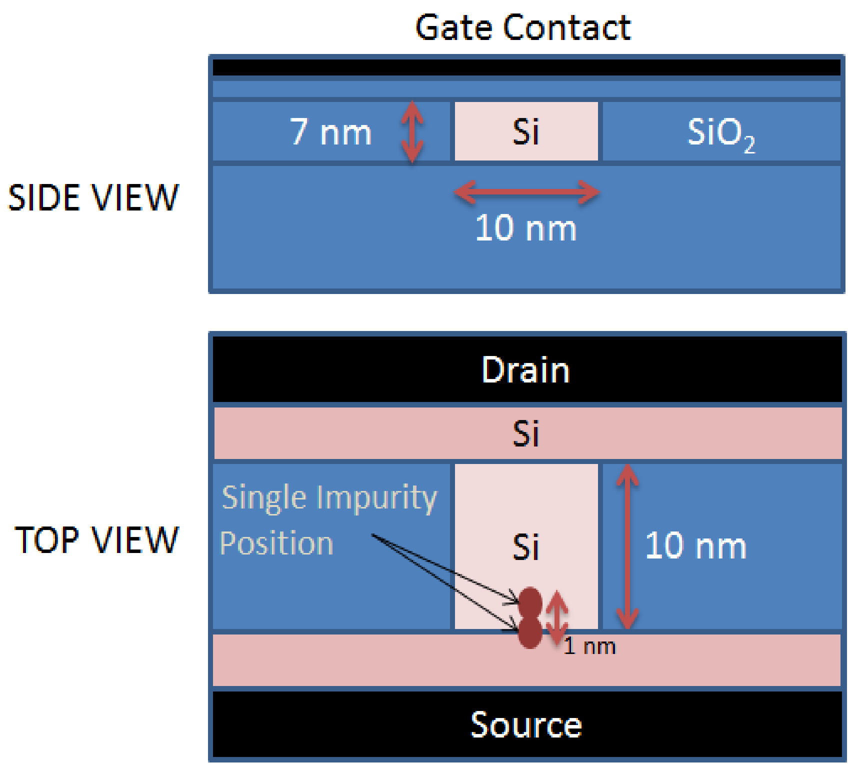
Convergence plot





D. Vasileska, A. Hossain and S. M. Goodnick, *ECS Transactions*, Volume 31, No. 1, pp. 83-91 (September 2010).

Nanowires – Unintentional Dopant



SINGLE IMPURITY IMPACT

GUMMEL CYCLE	No impurity case [µA/µA]	Source Edge [µA/µA]	1 nm Towards Drain [µA/µA]
1	4154	4122	4075
3	4068	4030	3974
5	4052	4035	3968
Degradation	N/A	0.47%	2.12%

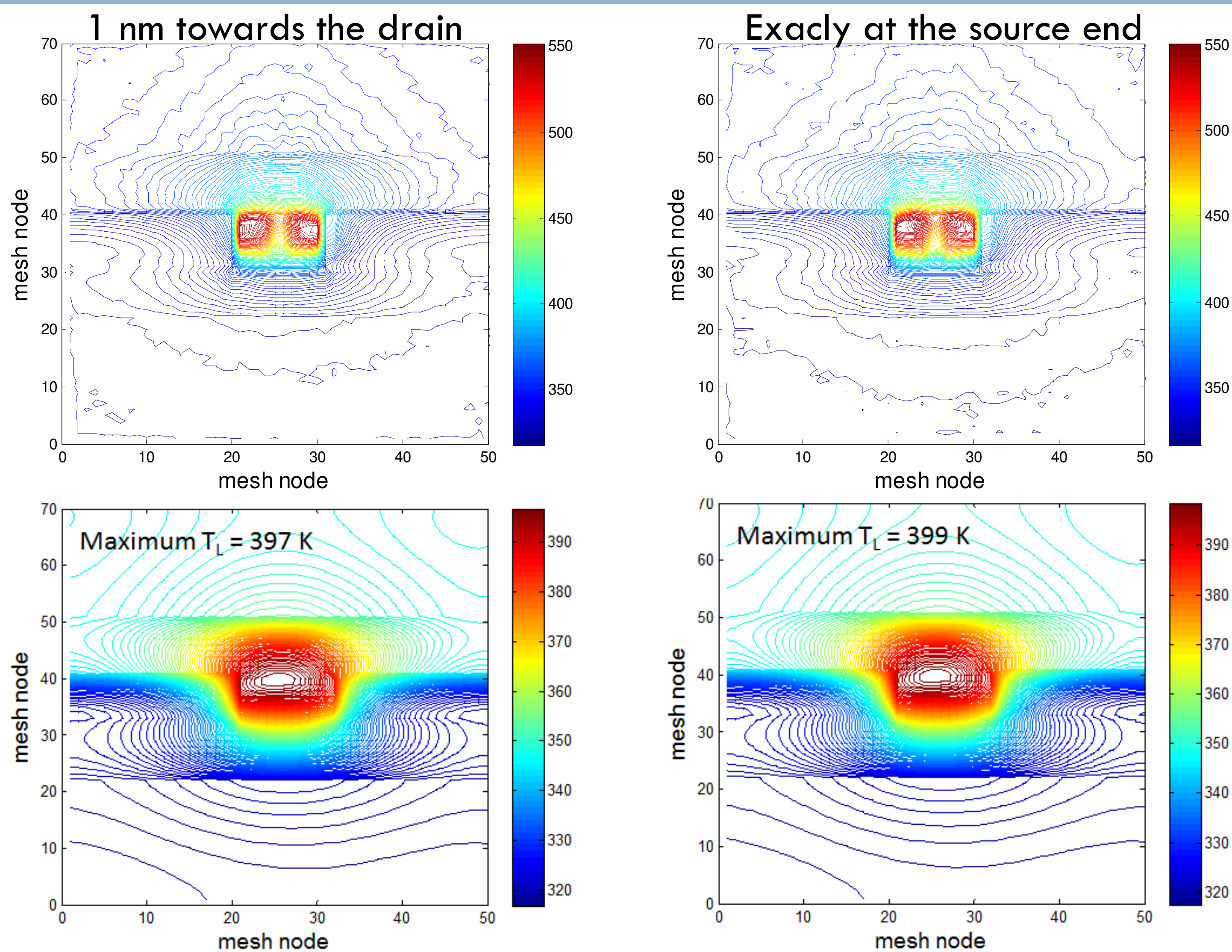
Screening of the source charges Reduces the impact of the negative trap.

Maximal impact

Unintentional Dopant

optical

acoustic

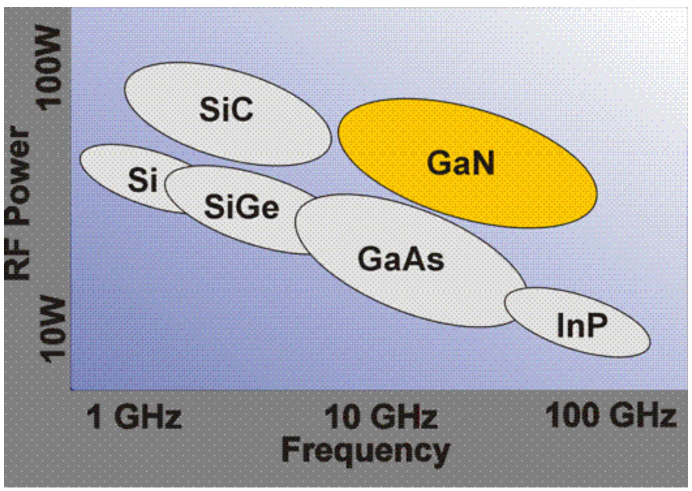


GaN HEMTS

Rainbow Bridge, Arizona

Simulation Results: GaN HEMTs

- Why GaN HEMTs?

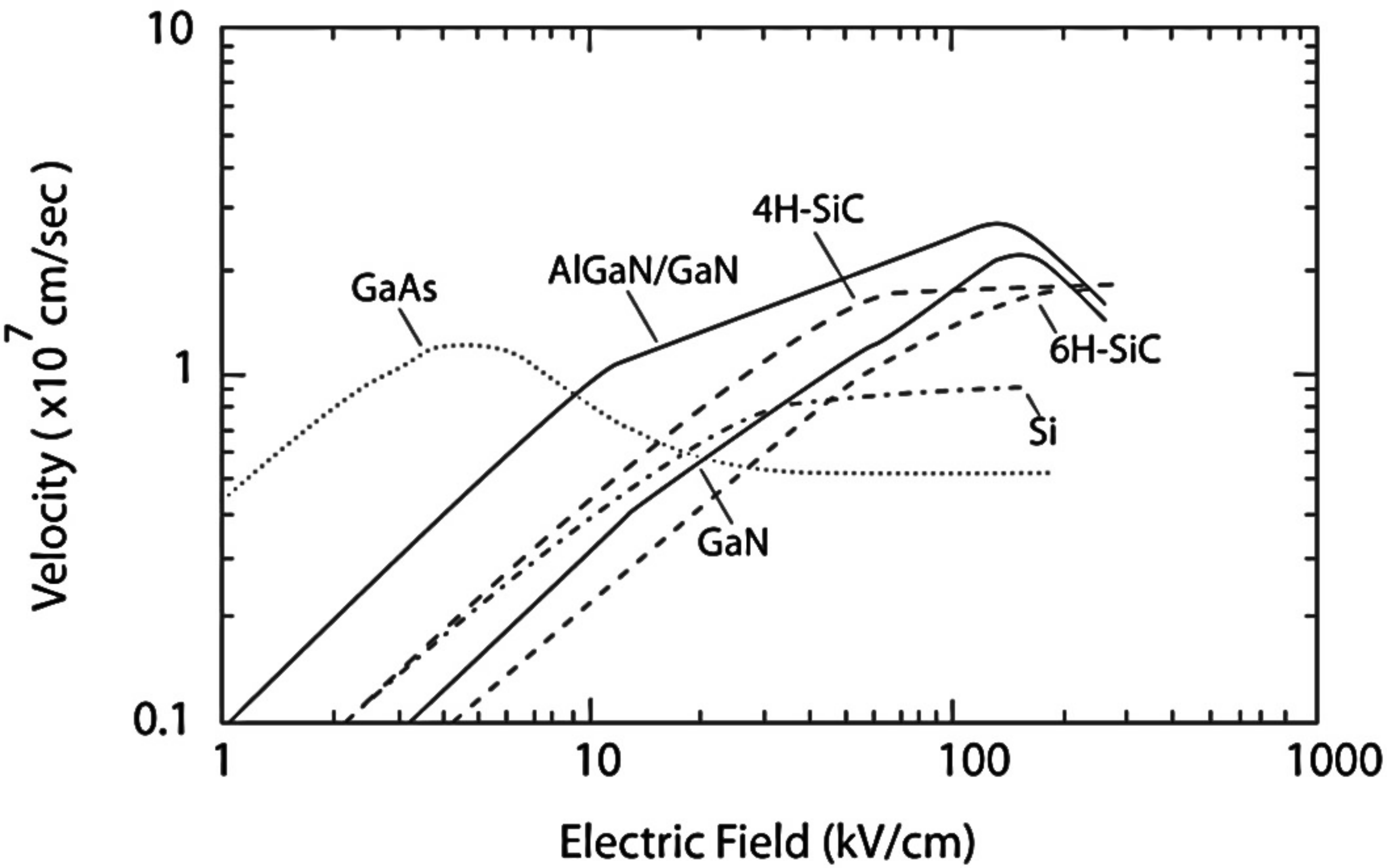


Where Gallium Nitride Outstrips Other Semiconductor Materials

Semiconductor (commonly used compounds)		Silicon	Gallium arsenide (AlGaAs/InGaAs)	Indium phosphide (InAlAs/InGaAs)[a]	Silicon carbide	Gallium nitride (AlGaN/GaN)
Characteristic	**Unit**					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm2/Vs	1500	8500	5400	700	1000-2000
Saturated (peak) electron velocity	$X10^7$ cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0
Thermal conductivity	W/cm•K	1.5	0.5	0.7	4.5	>1.5
Relative dielectric constant	ε_r	11.8	12.8	12.5	10.0	9.0

[a] The compounds are loosely known as indium-based.

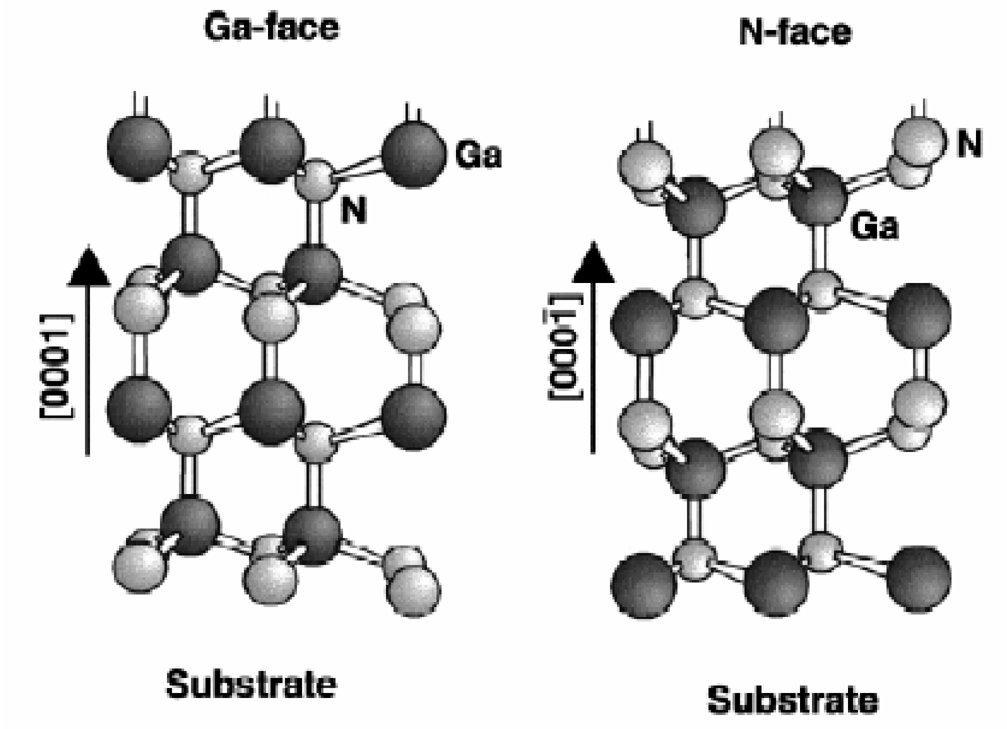
GaN HEMTs …



10
1
0.1
1
10
100
1000
Velocity (x10^7 cm/sec)
Electric Field (kV/cm)
GaAs
AlGaN/GaN
4H-SiC
6H-SiC
Si
GaN

GaN HEMTs …

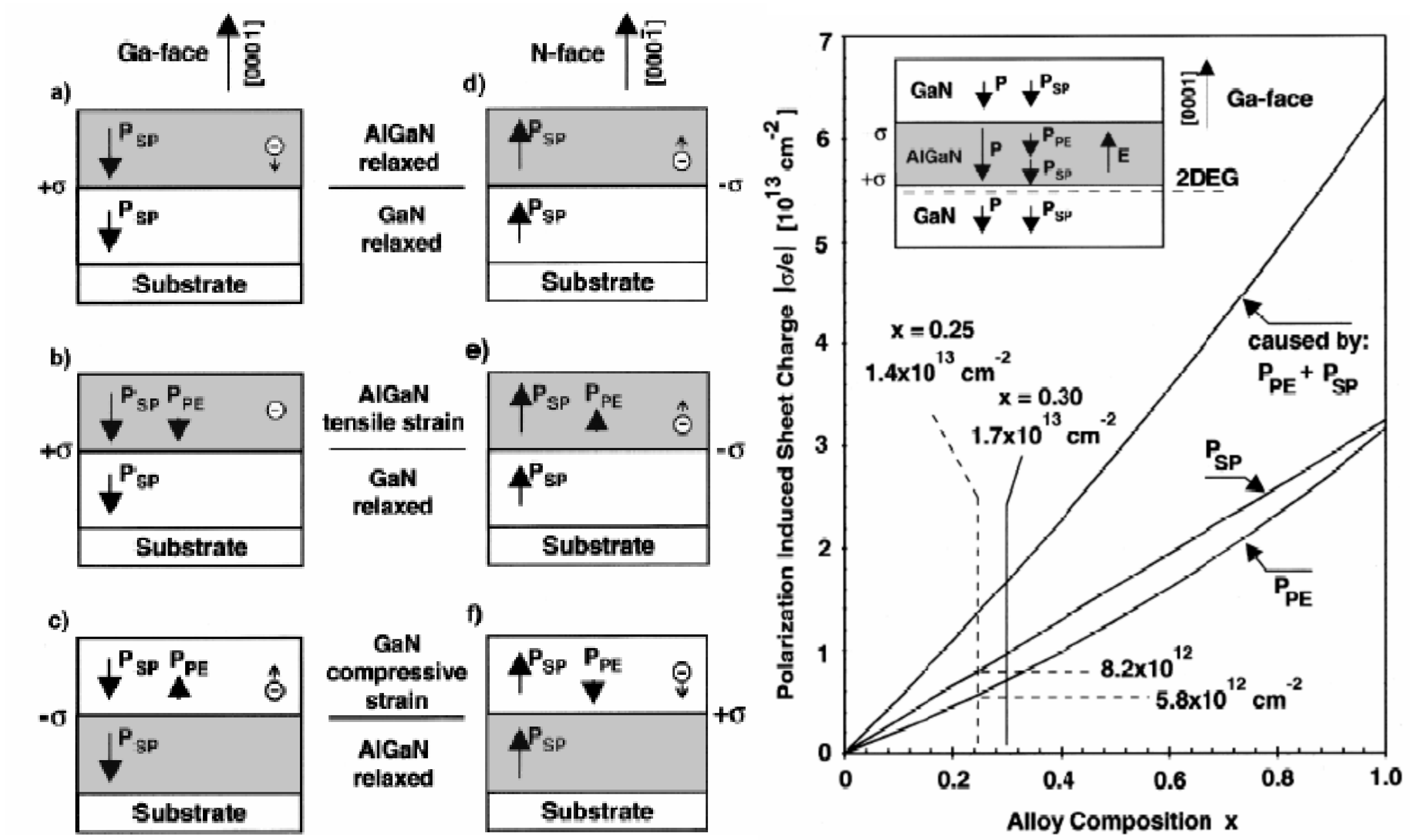
- Wurtzite AlGaN/GaN



AlGaN/GaN grown on sapphire by MOCVD is always Ga-faced, but material grown by MBE can have either Ga- or N-faced surface depending on the existence of AlN nucleation layer.

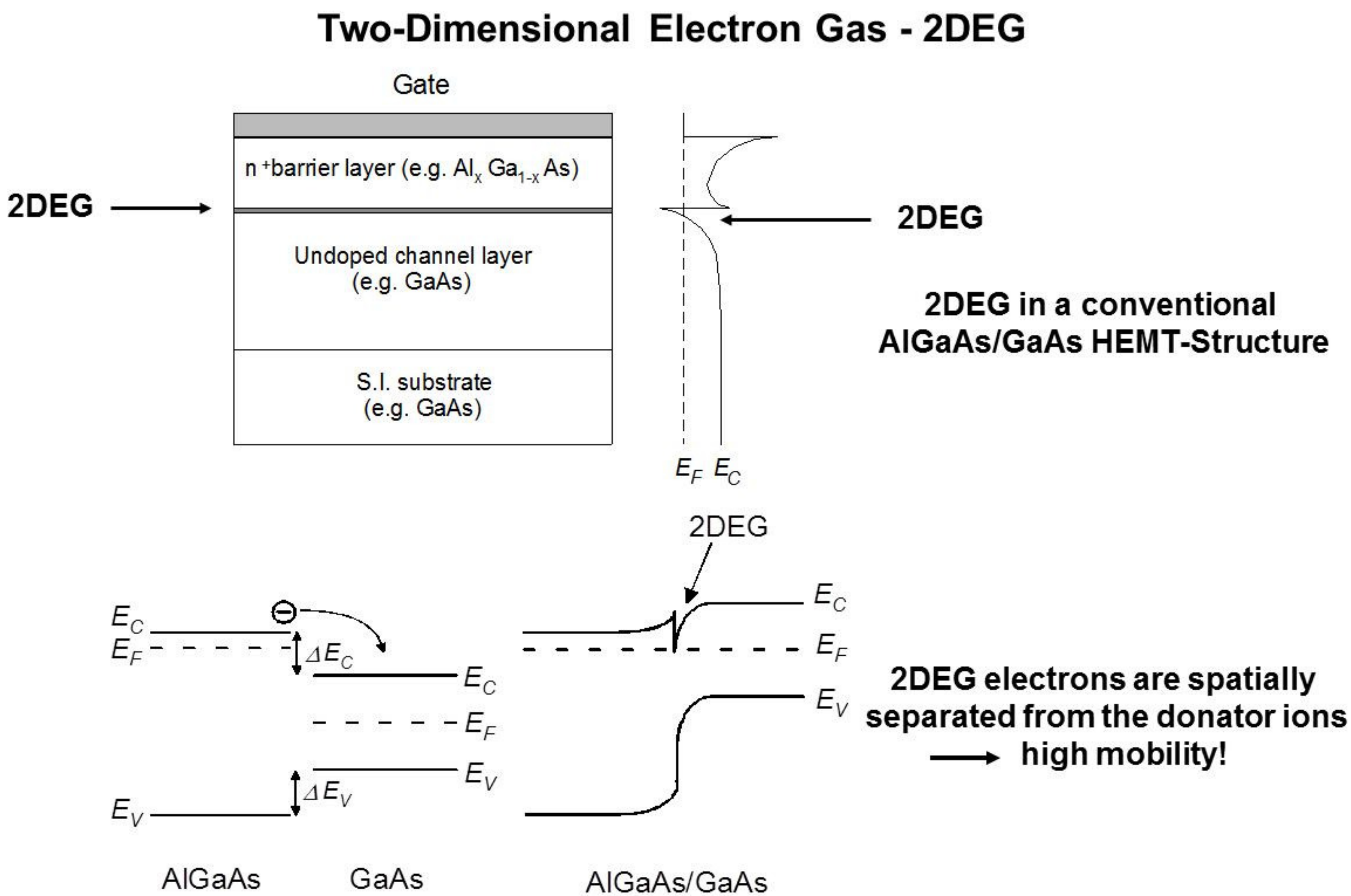
GaN HEMTs …

- Spontaneous and Piezoelectric Polarization Charge



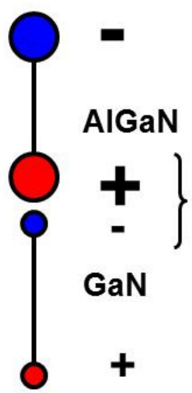
GaN HEMTs …

- Comparison to GaAs devices



GaN HEMTs …

- What is different in GaN HEMTs …

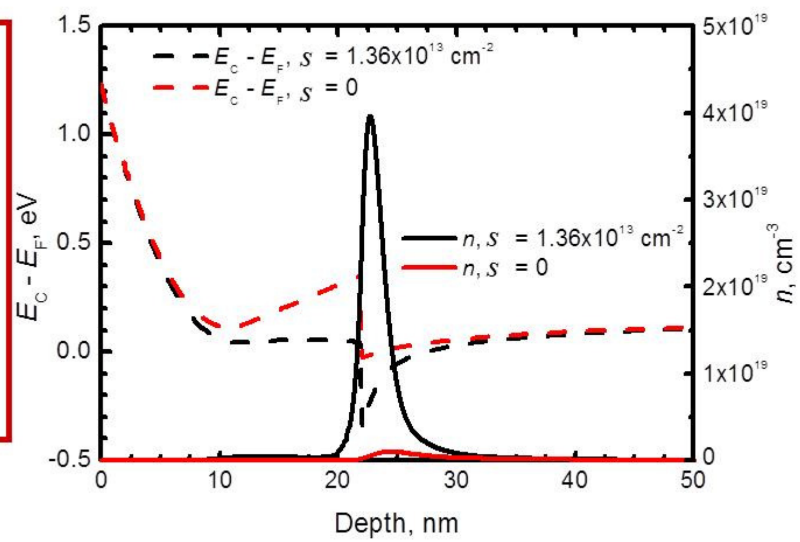


At the AlGaN/GaNinterface occurs a positive net charge

+ σ leading to the formation of a 2DEG in the GaN.

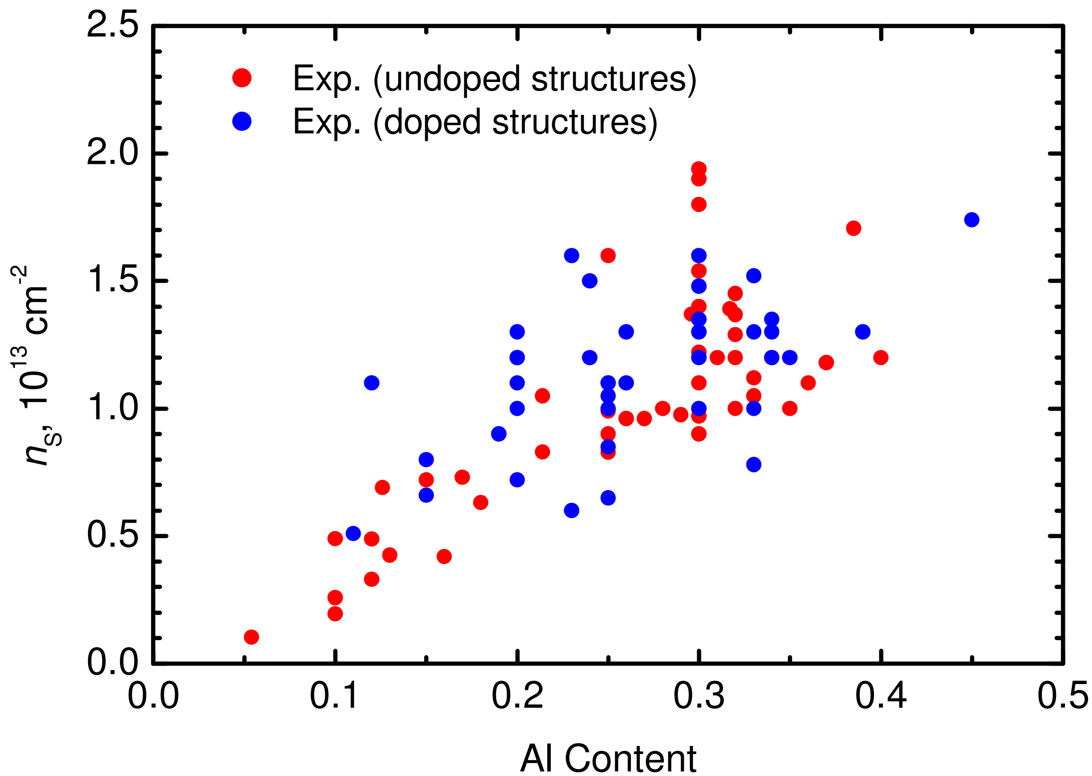
Two important messages:

- **Only a small portion of the 2DEG elecrons is caused by the barrier doping !**
- **Even without any doping very high 2DEG sheet concentrations are possible!**



GaN HEMTs …

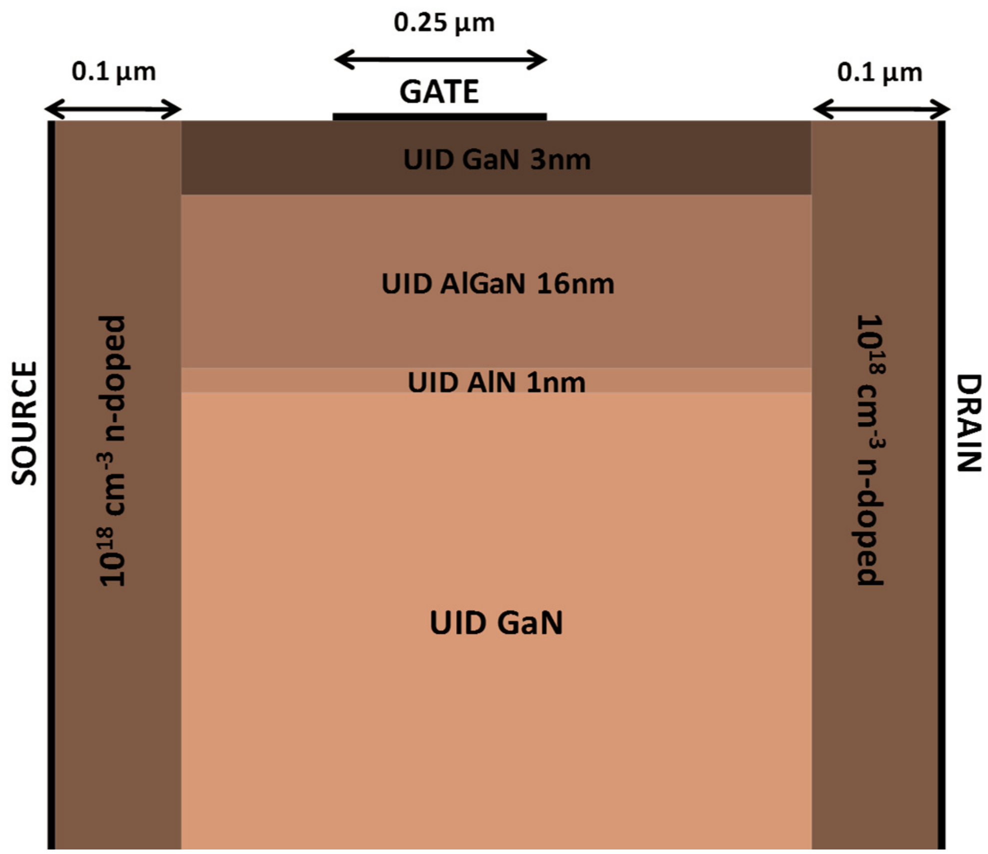
- Large sheet electron densities



Measured 2DEG sheet concentration n_S in $Al_xGa_{1-x}N/GaN$ heterostructures vs. Al content x

GaN HEMTs …

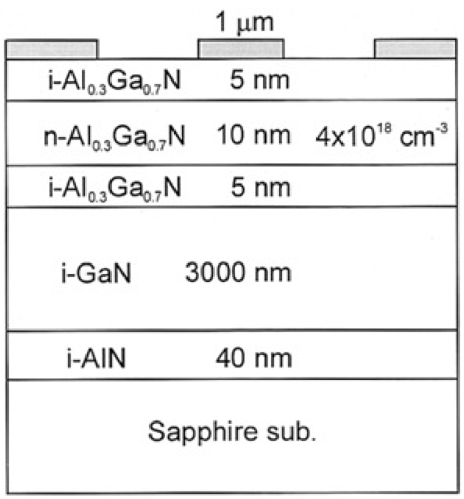
- Device Structure



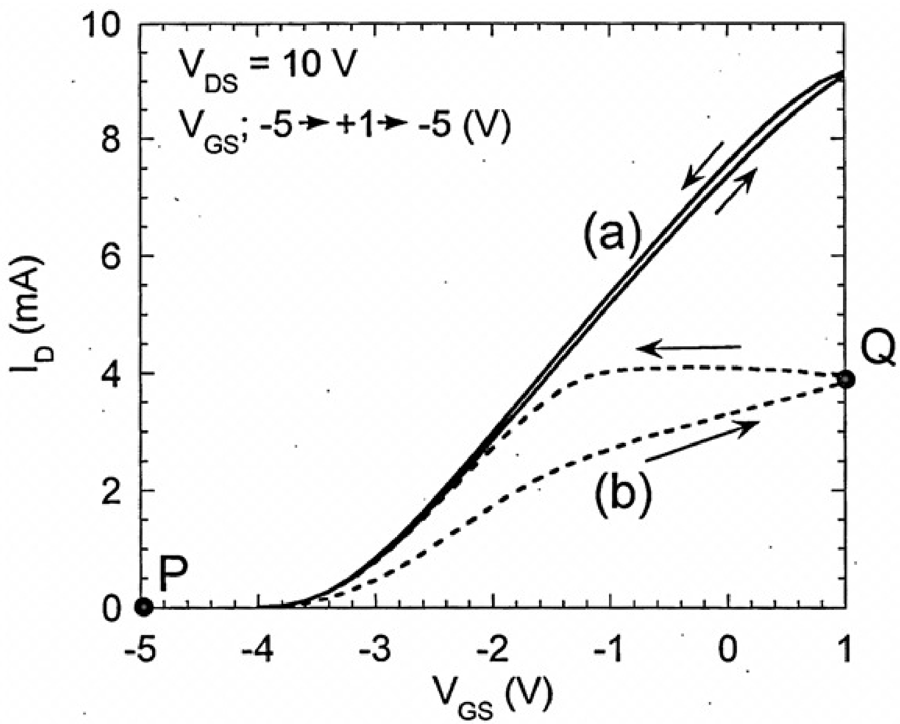
Device Structure Provided by Jesus del Alamo, MIT.

GaN HEMTs …

- Current Collapse



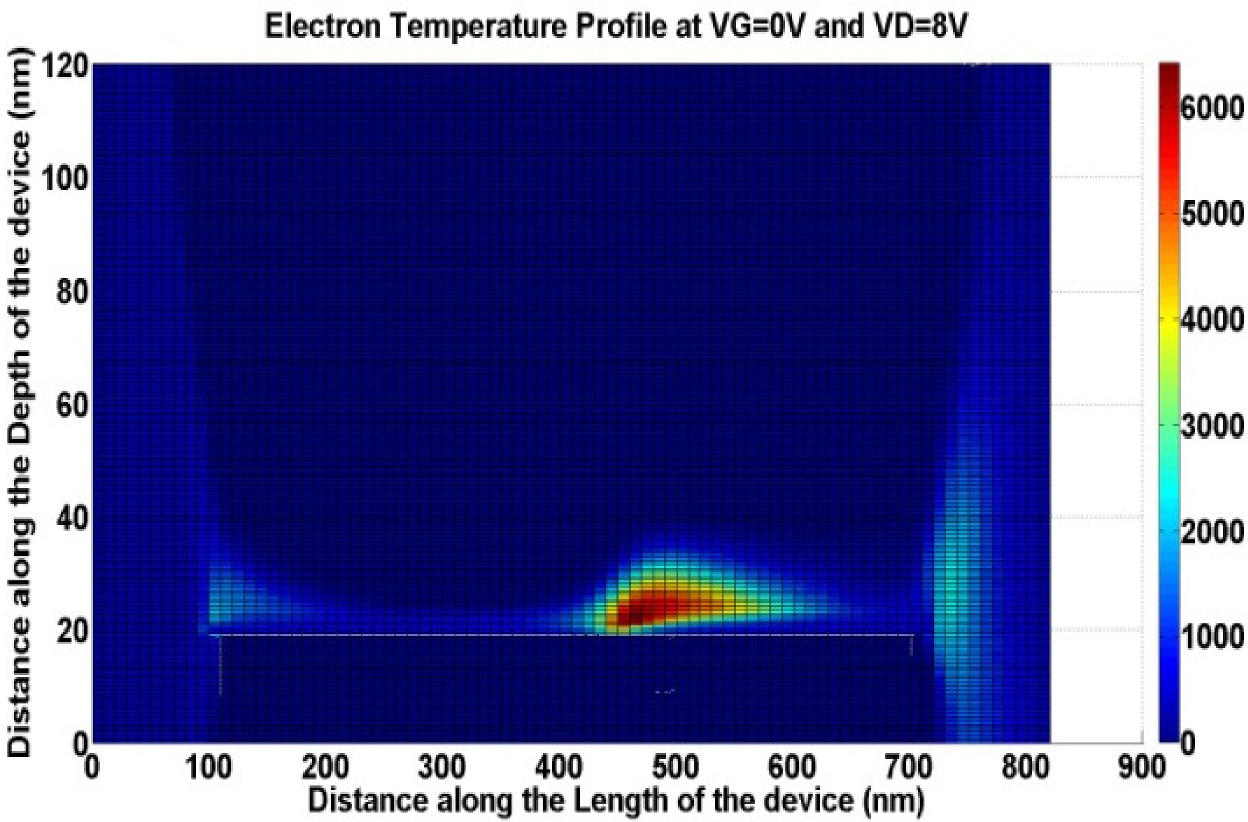
Transfer characteristics (a) before and (b) after gate bias stress. The Stress condition is V_{GS}=-5V and V_{DS}=10V.



Takashi Mizutani, Yutaka Ohno, M. Akita, Shigeru Kishimoto, and Koichi Maezawa, *IEEE Trans. Electron Devices, Vol. 50, 2015 (2003).*

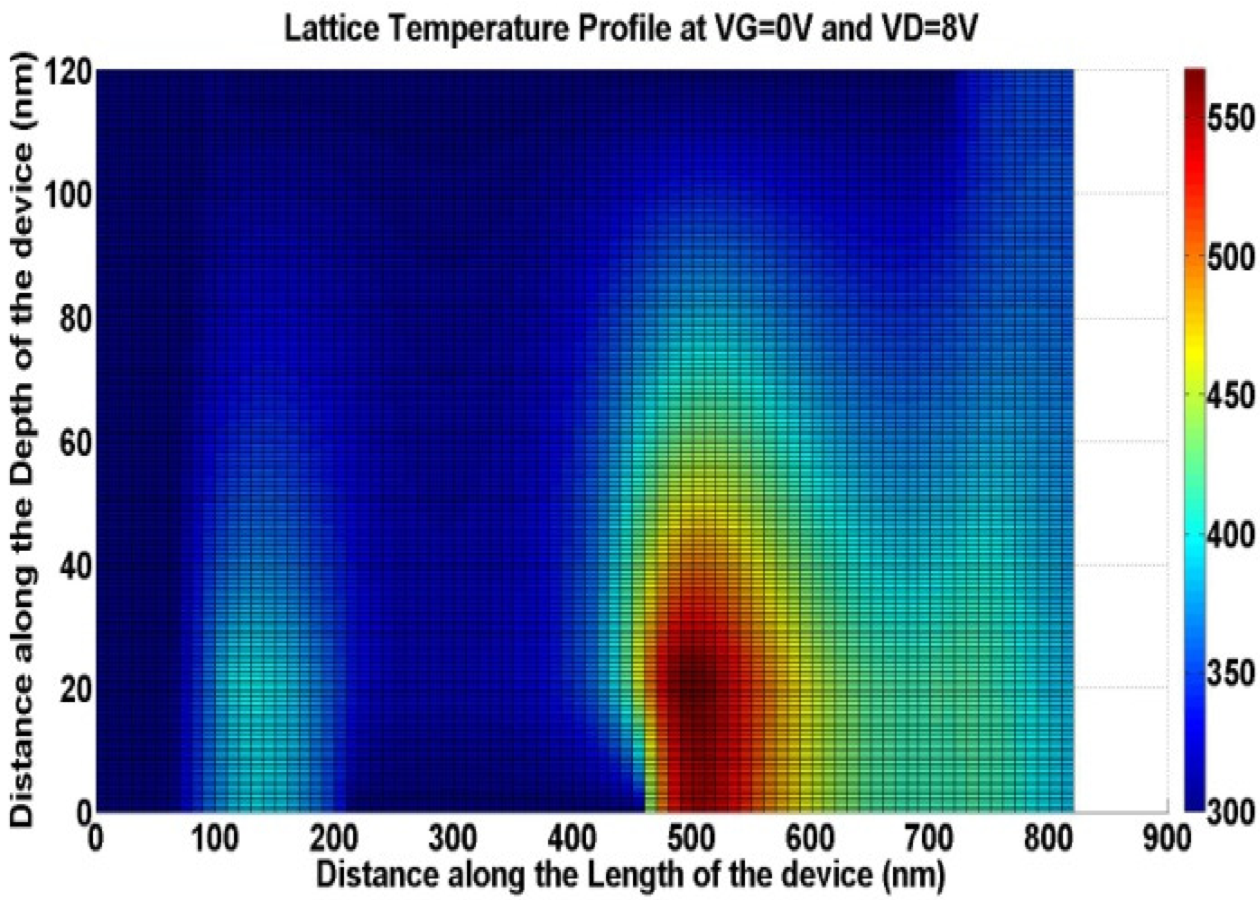
GaN HEMTs …

- Is Self-Heating Contributing to the Current Collapse?



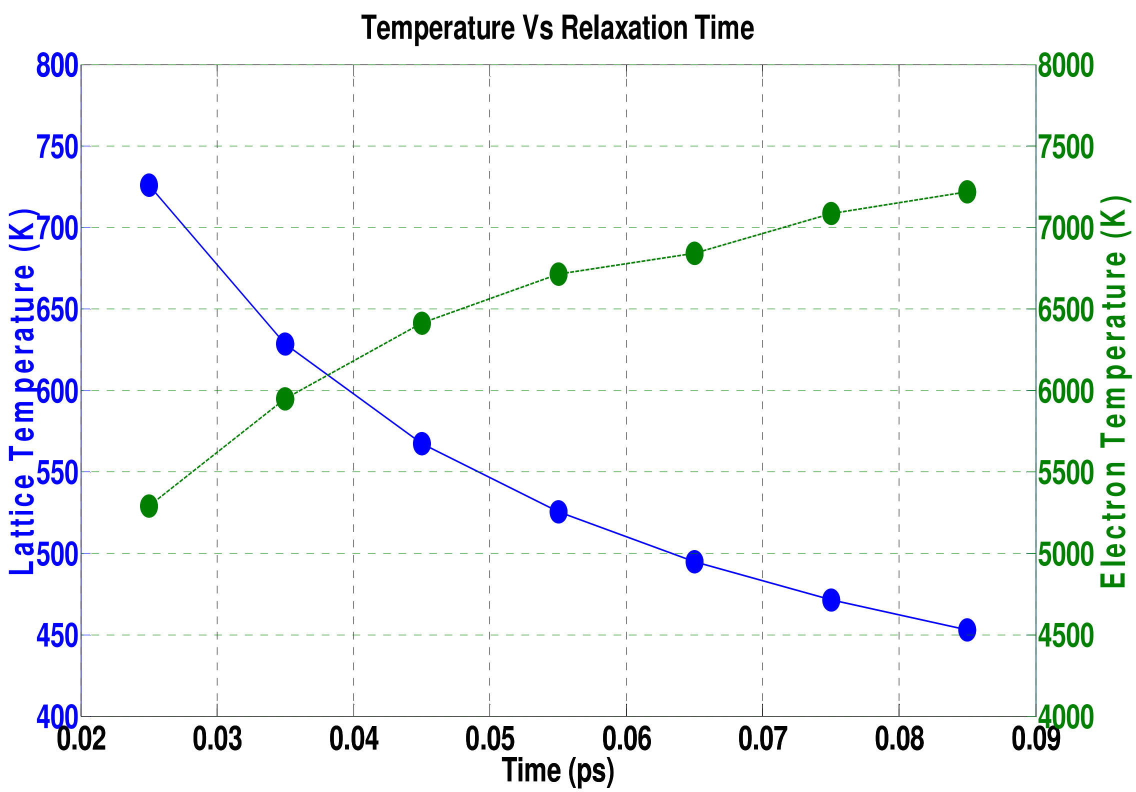
GAN HEMTs …

- Lattice Temperature



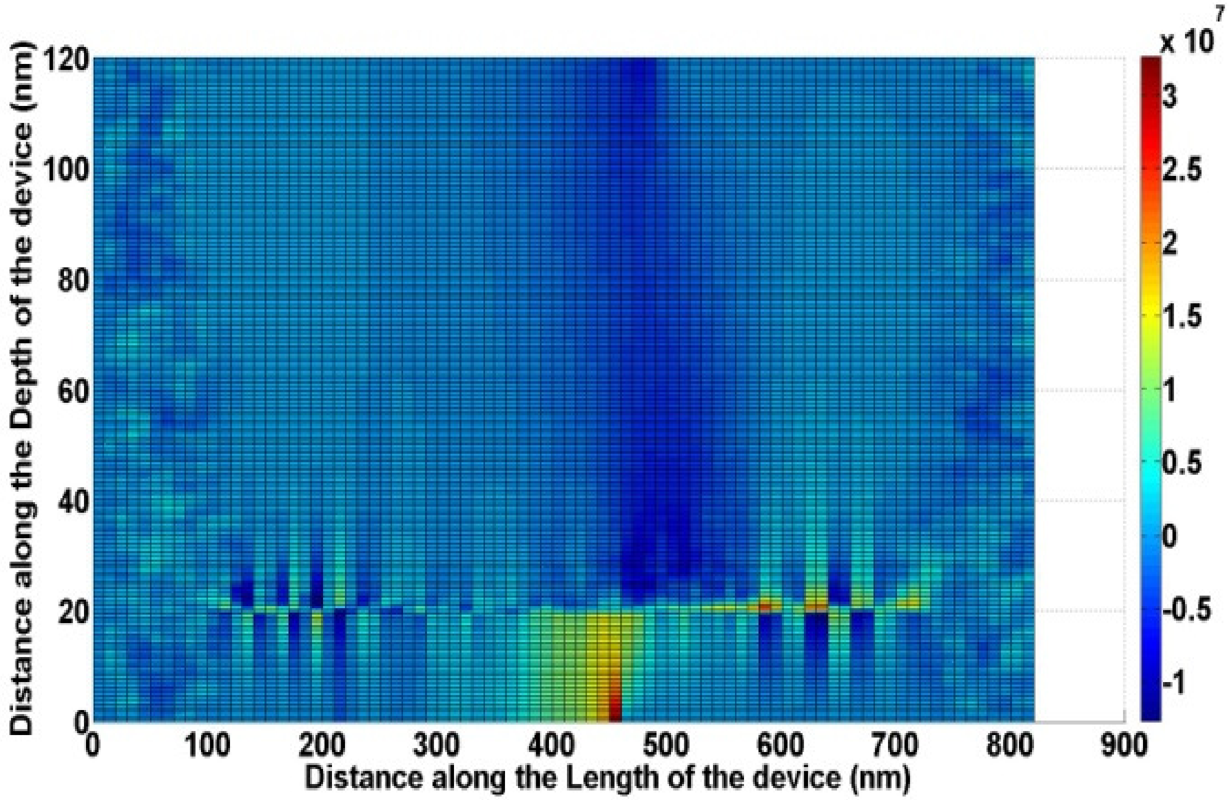
GAN HEMTs …

- Peak Electron and Lattice Temperatures



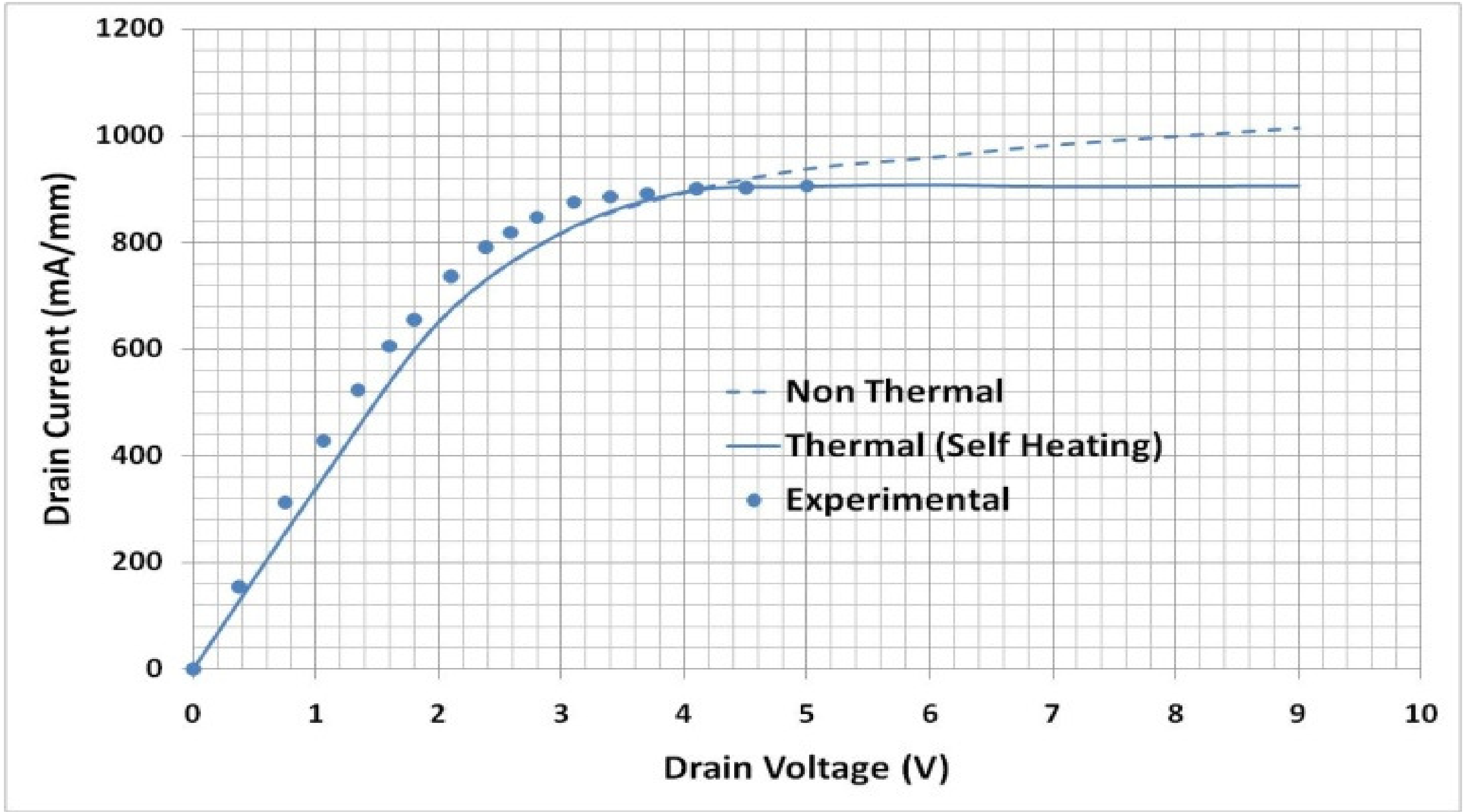
GAN HEMTs …

- Electric Field Change

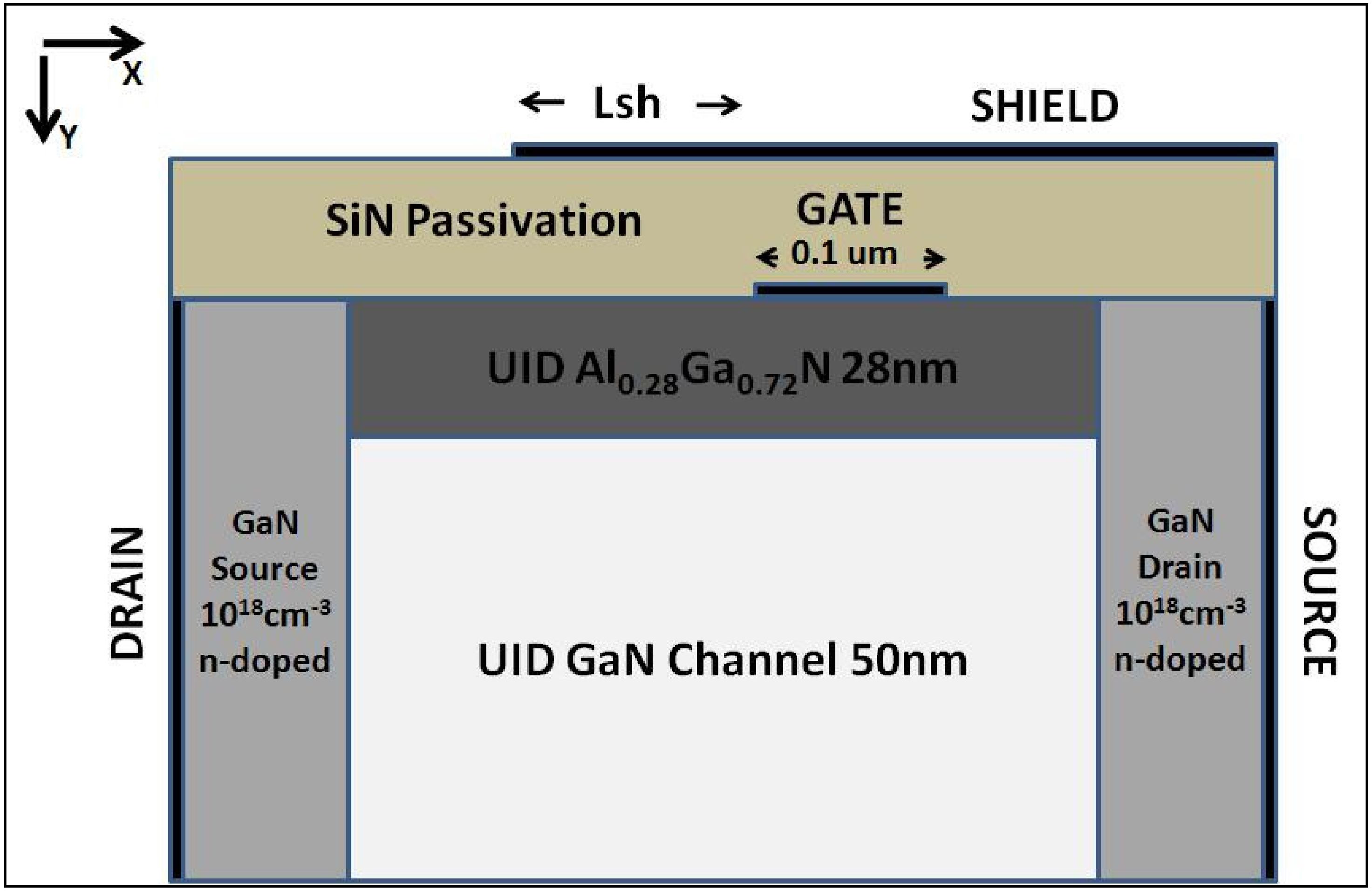


GAN HEMTs …

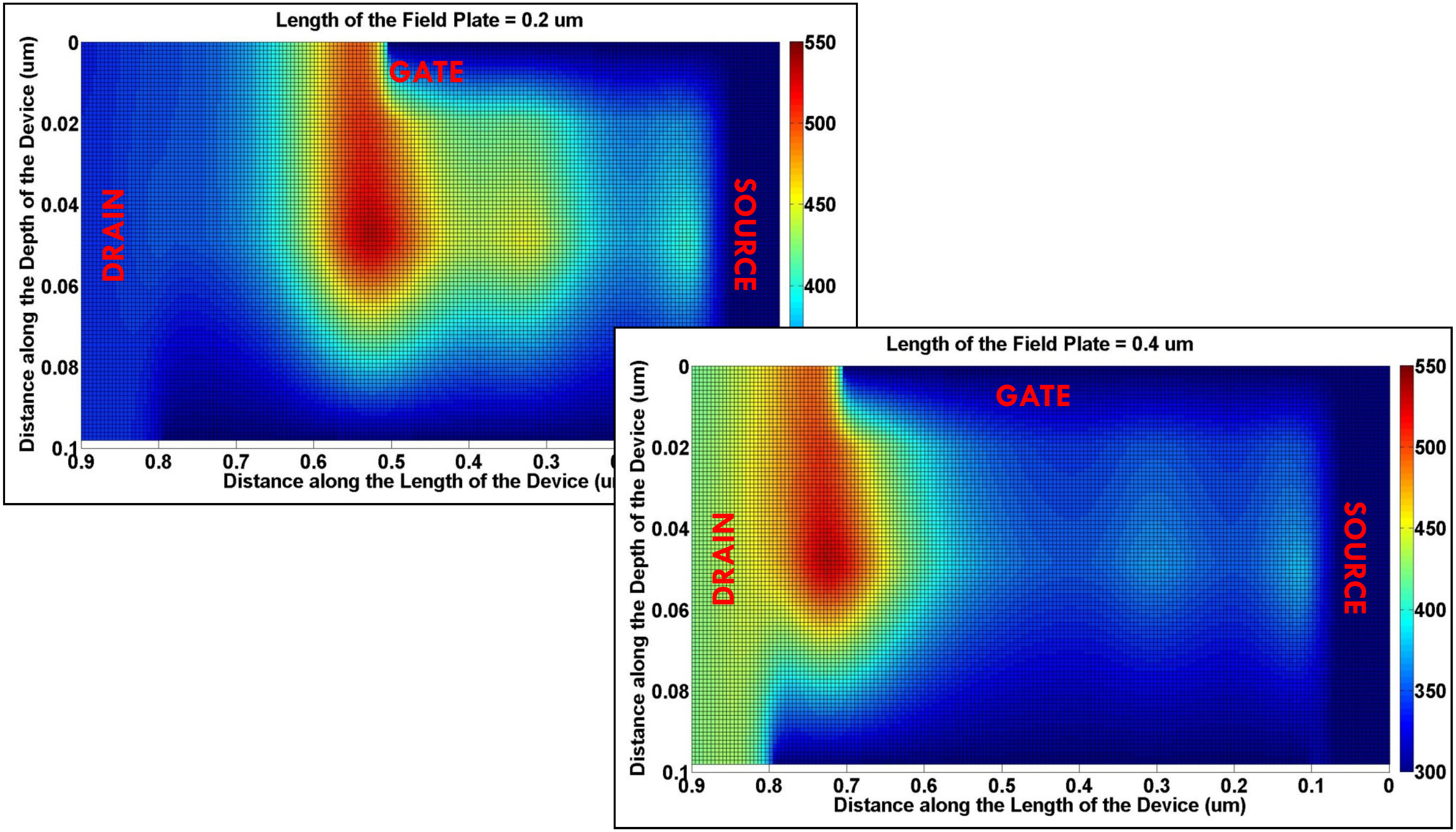
- Current Degradation



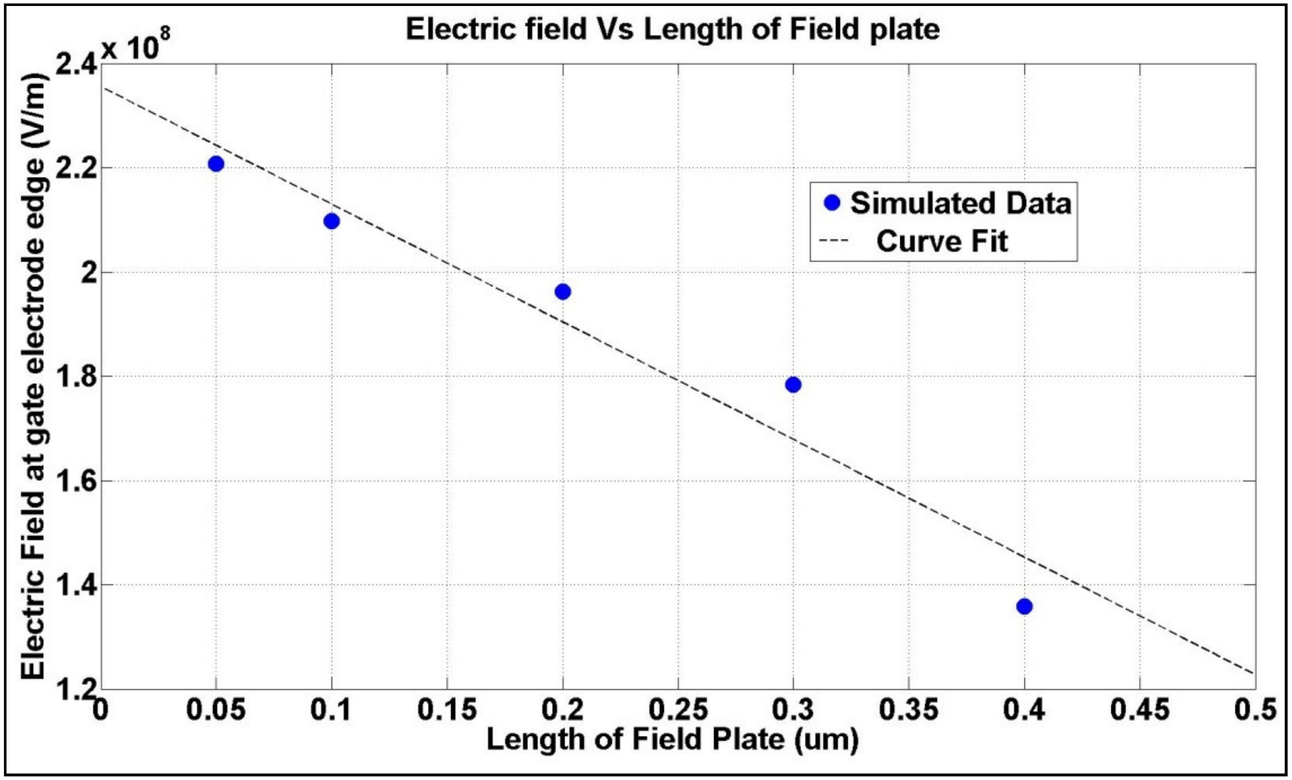
The Role of Shielding Electrode



The Role of Shielding Electrode …

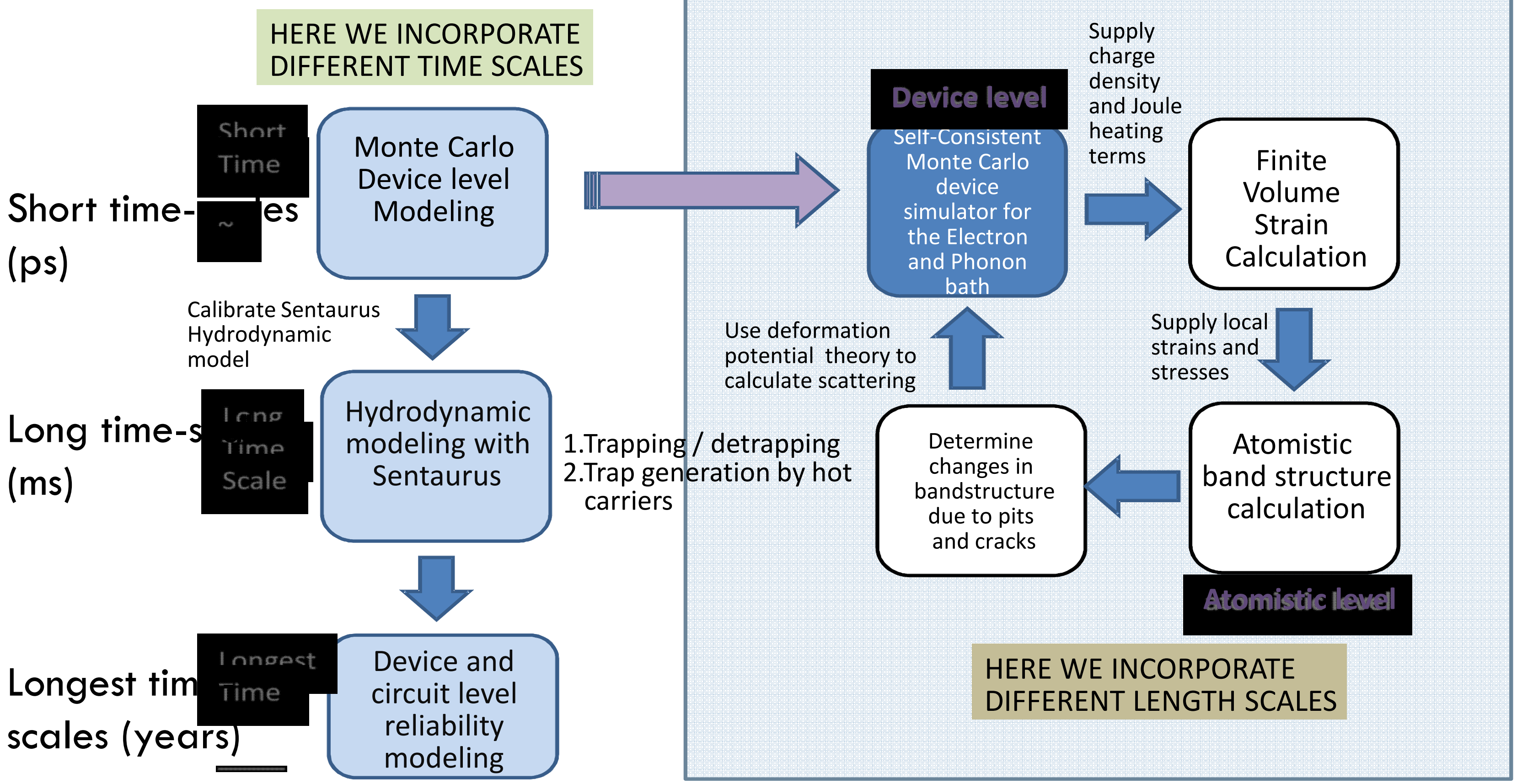


The Role of Shielding Electrode …



GAN HEMTs …

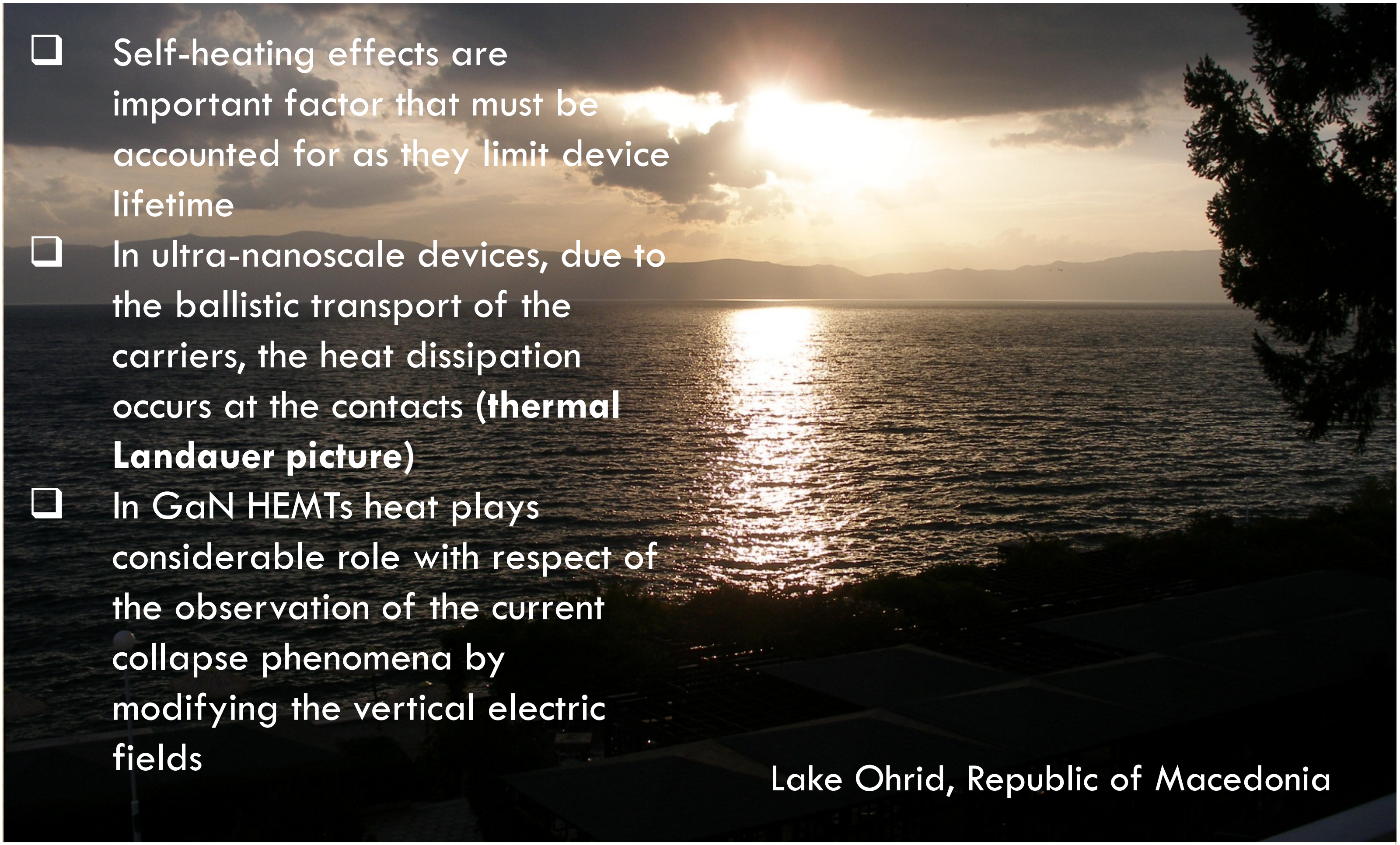
- Multi-Scale Modeling



Currently supported by ARL

Conclusions

- Self-heating effects are important factor that must be accounted for as they limit device lifetime
- In ultra-nanoscale devices, due to the ballistic transport of the carriers, the heat dissipation occurs at the contacts **(thermal Landauer picture)**
- In GaN HEMTs heat plays considerable role with respect of the observation of the current collapse phenomena by modifying the vertical electric fields



Lake Ohrid, Republic of Macedonia

Thanks to …

Army Research Laboratory	National Science Foundation